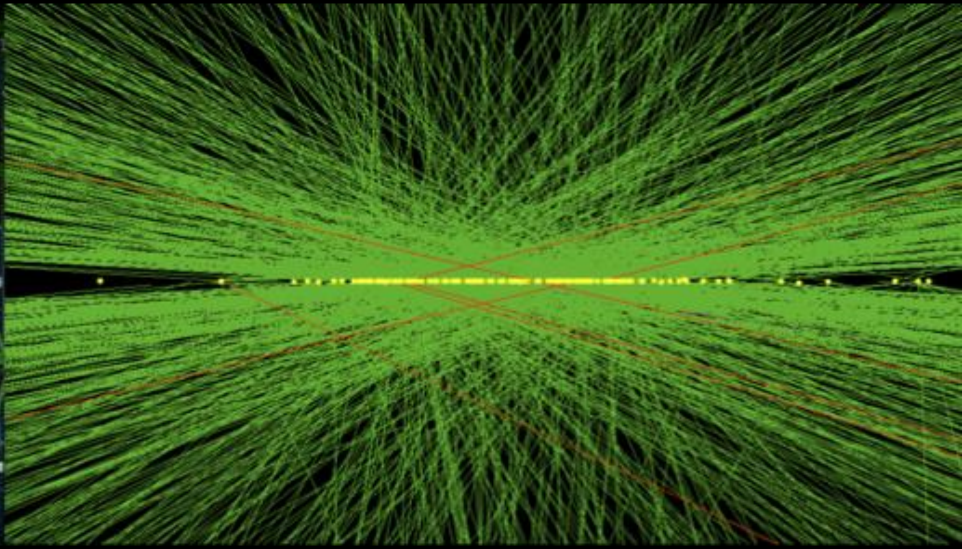


Trigger Electronics & Data Acquisition

Focus: Large Hadron Collider Experiments

Sridhara Dasu

UNIVERSITY OF WISCONSIN–MADISON

Original slides & graphics "stolen" from:
Wesley Smith, Sergio Cittolin, Tom Gorski, Ales Svetek, Maria Cepeda, Sascha Savin, Varun Sharma, Piyush Kumar, Pallabi Das, Isobel Ojalvo, Kevin Stenson, Phil Harris, …

Trigger on interesting events quickly using partial data

Store complete data for detailed processing offline

The Scientific Process

The Detector

Trigger Electronics & Data Acquisition

Software & Computing

SCIENCE

Journal Publications

Petabyte per second

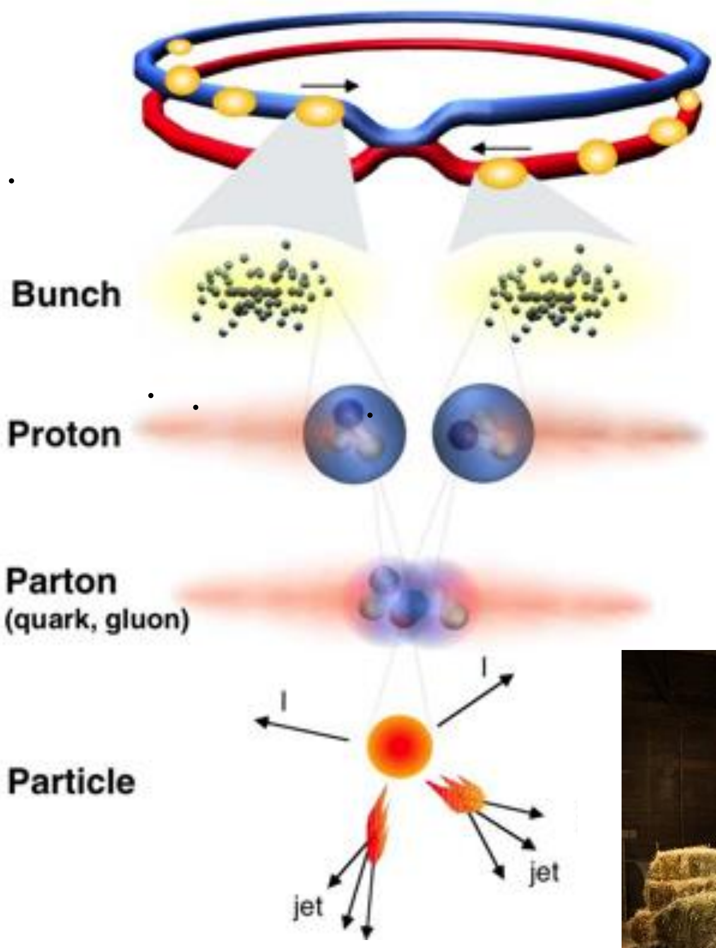
Petabytes per year

Petabytes get reduced to a social media post!

will.i.am @iamwill · Jul 4, 2012

Happy 4th of july to all americans...& happy "god particle" day to science enthusiast...congrats to all the scientist at cern...#willpower

Proton-Proton Collisions at the LHC

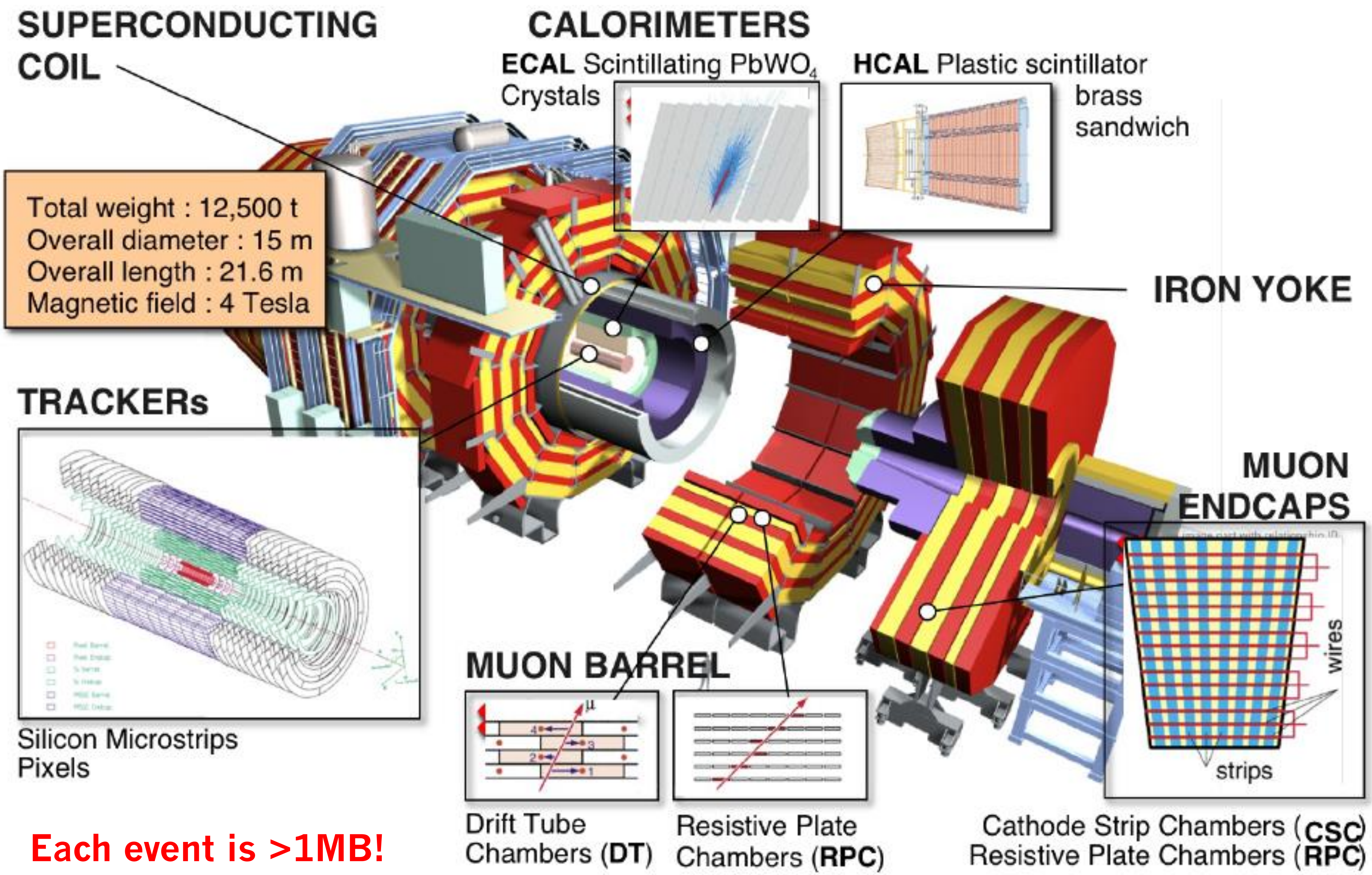


	Run-2	Run-1
Beam energy	6.5 TeV	4.0 TeV
Bunches/ beam	2556	1380
Protons/ bunch	2.5×10^{11}	2.2×10^{11}
N pp Collisions Created	$\sim 10^{16}$	3.5×10^{14}
N Higgs Events	$\sim 10^{4}$	~few 10^{2}

Fetch me my needle buried in those hay stacks –
And, do it
As Soon As Possible

1 event in 10 000 000 000 000 !

CMS, an LHC Detector



Each event is >1MB!

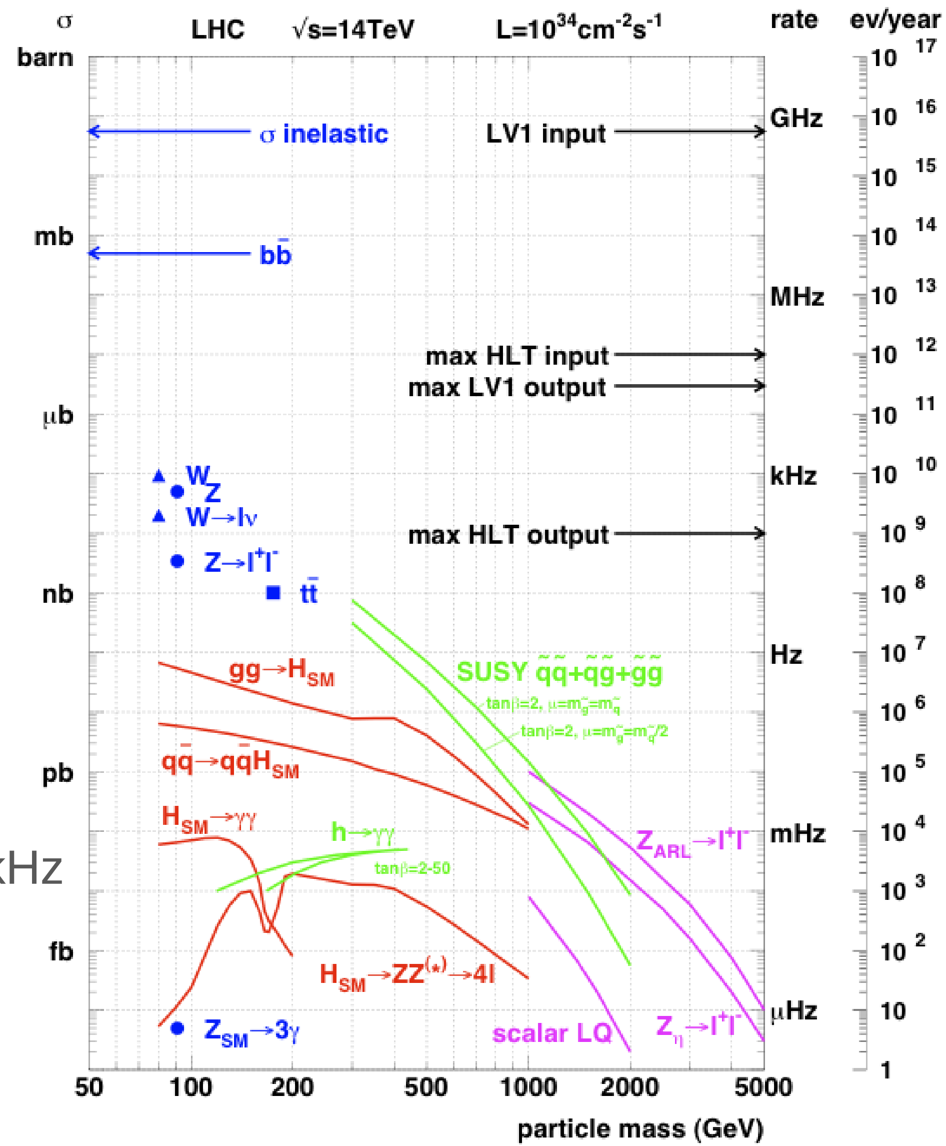
$L = 2 \times 10^{34} cm^{-2}s^{-1}$

- 50 pp events/25 ns crossing
  - ~ 1 GHz input rate
  - "Good" events contain ~ 50 background overlap
- 1 kHz W events
- 10 Hz top events
- < 10^4 detectable Higgs/year

Can store ~ 1000 Hz events

Select in stages

- Level-1 Triggers
  - 1 GHz (pp-interactions) to 100 kHz
- High Level Triggers
  - 100 kHz to 1000 Hz



Collisions (p-p) at LHC

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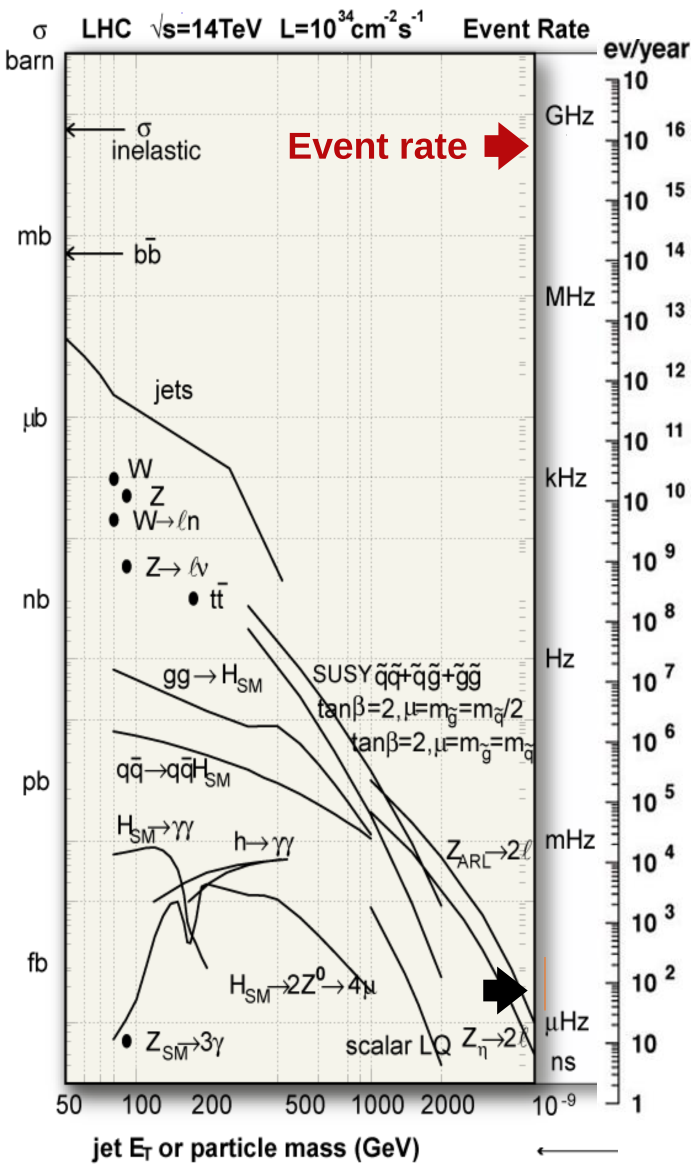
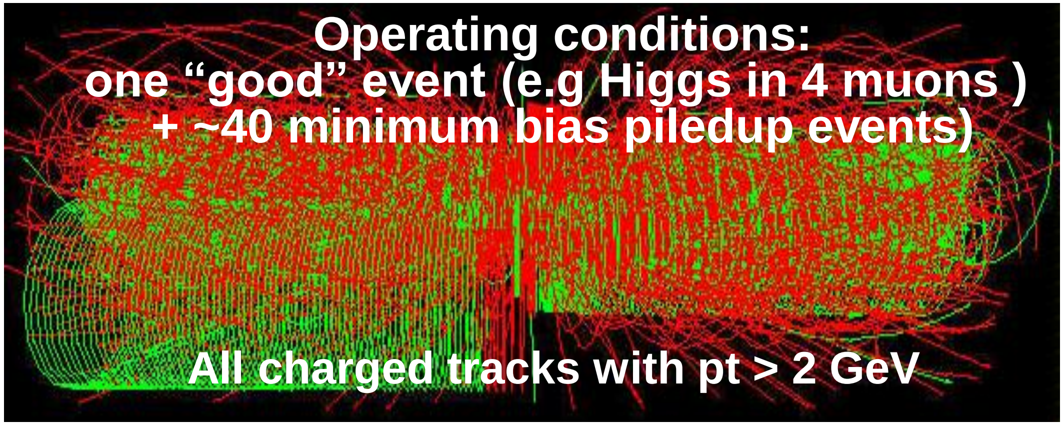
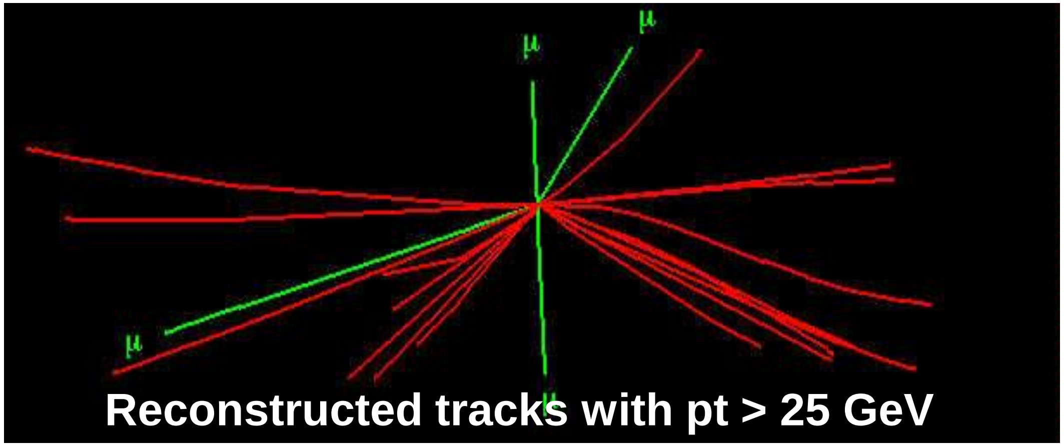




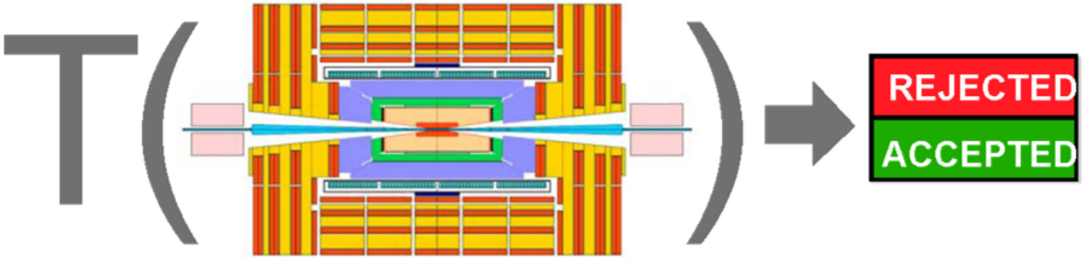


Event size:	**~ 1 M bytes**
Event Rate:	**~ 32 M Hz**

Trigger Task – Quick Complex Decision

- **Task: inspect detector information and provide a first decision on whether to keep the event or throw it out**

The trigger is a function of :



Event data & Apparatus
Physics channels & Parameters

- **Detector data not (all) promptly available**
- **Selection function highly complex**

⇒T(...) is evaluated by successive approximations, the

TRIGGER LEVELS

(possibly with zero dead time)

(HL) LHC Physics – Trigger Challenge

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Low ≅ 30 GeV

Electroweak Symmetry Breaking Scale

Low P_T γ, e, μ

- **Higgs (125 GeV) studies and higgs sector characterization**
- **Quark, lepton Yukawa couplings to higgs**

Low P_T B, τ jets

New physics at TeV scale to stabilize higgs sector

- **Spectroscopy of new EWK produced resonances (SUSY or otherwise)**

Multiple low P_T objects

- **Find dark matter candidate**

Missing E_T

Multi-TeV scale physics (loop effects)

- **Indirect effects on flavor physics (mixing, FCNC, etc.)**
  - B_s mixing and rare B decays

~ Dedicated triggers (CMS) or experiment (LHCB)

- **Lepton flavor violation**
  - Rare Z and higgs decays

Low P_T leptons

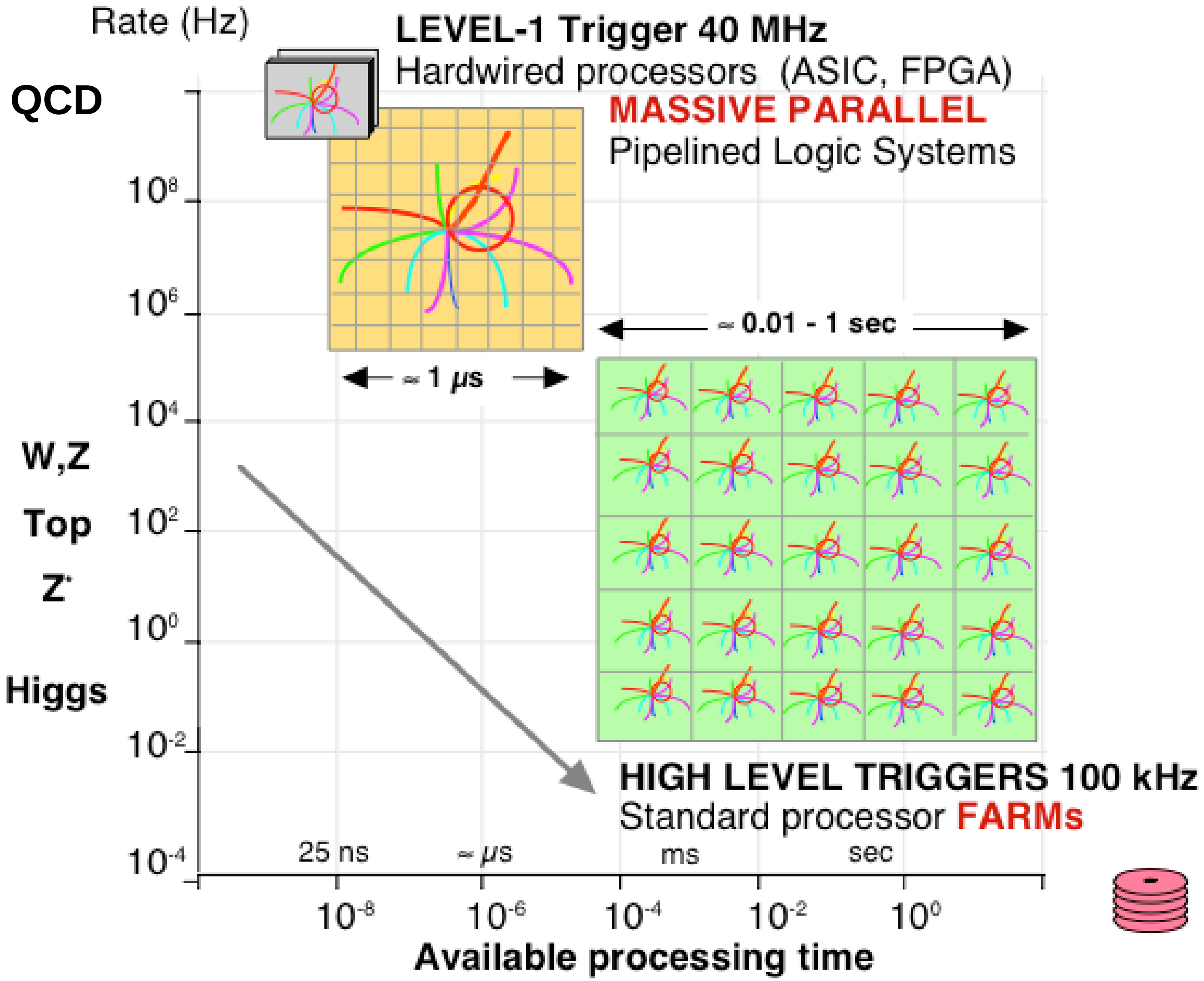
Planck scale physics

- **Large extra dimensions to bring it closer to experiment**
- **New heavy bosons**
- **Blackhole production**

High P_T leptons and photons

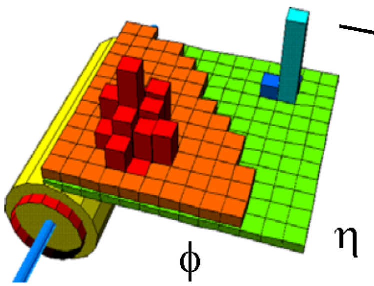
Multi particle and jet events

LHC Data Processing to Trigger



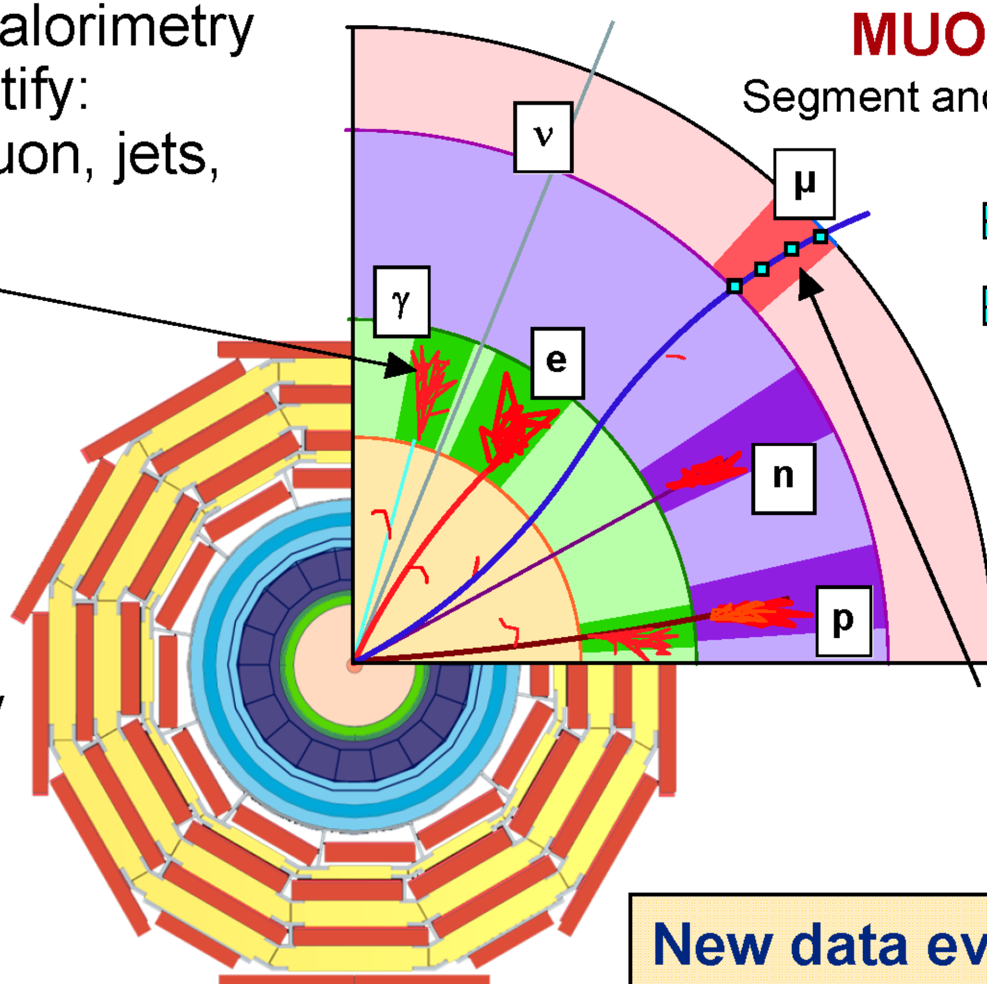
Level 1 Trigger Data

Use prompt data (calorimetry and muons) to identify:
High p_t electron, muon, jets, missing E_T



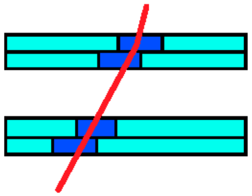
CALORIMETERs

Cluster finding and energy deposition evaluation



MUON System

Segment and track finding



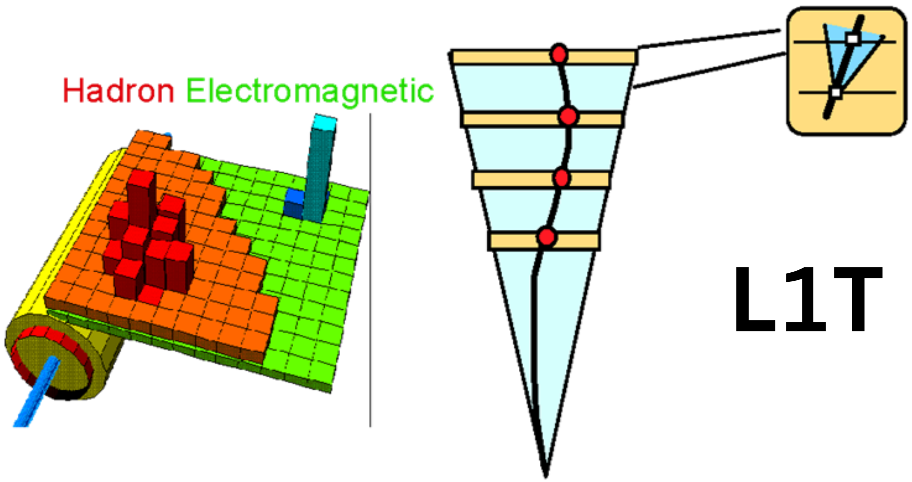
New data every 25 ns
Decision latency ~ μs

L1 @ LHC: Only Calorimeter & Muon

HLT@LHC: Key additional feature - Tracker

New tracker and level-1 track trigger envisioned for HL-LHC

- **Pattern recognition much faster/easier**

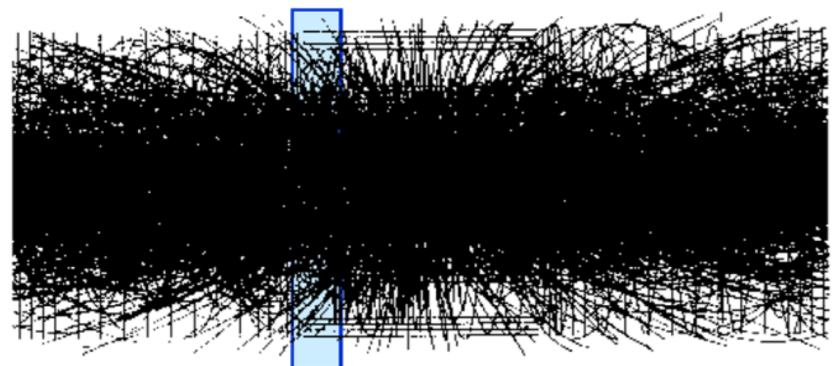


L1T

Simple Algorithms

Reduced amounts of data

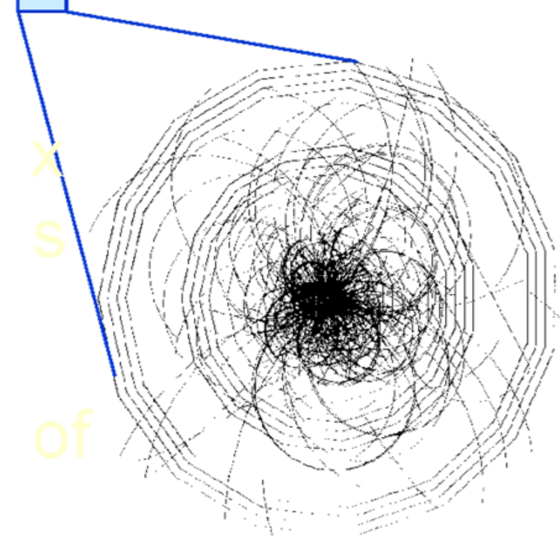
- **Compare to tracker info**



HLT

Complex Algorithms

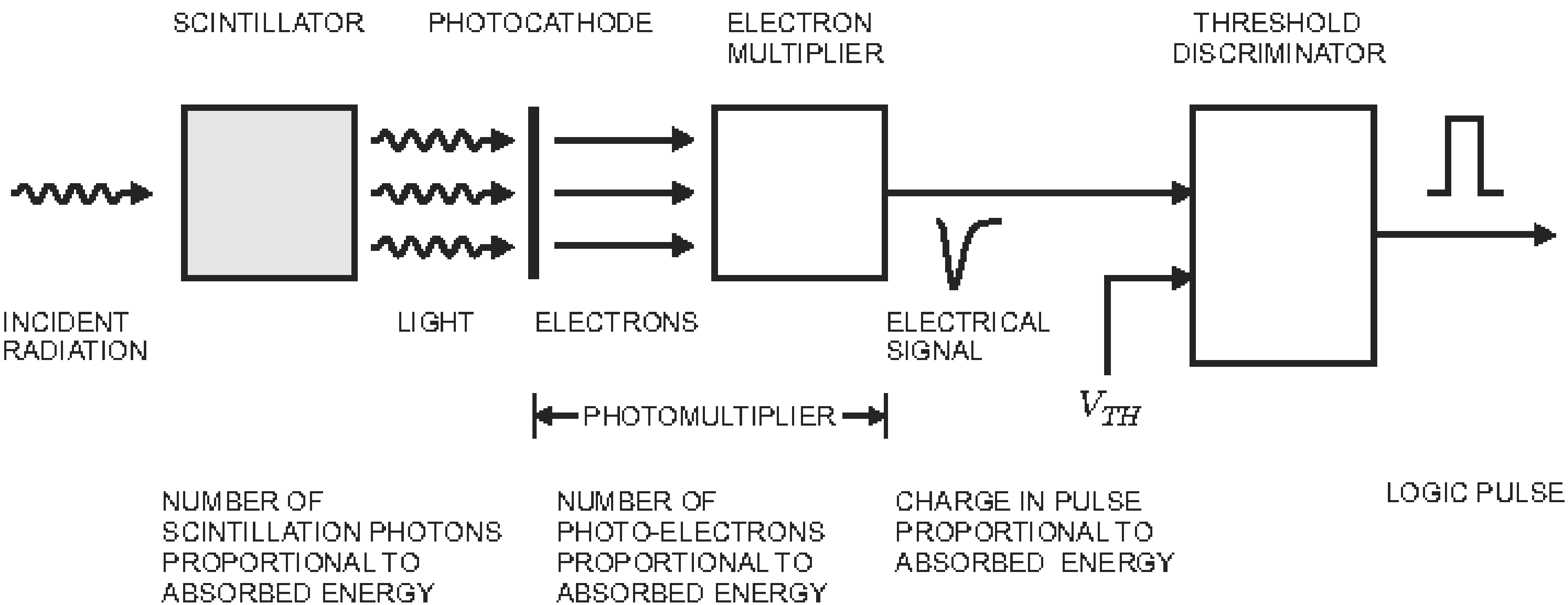
Huge amounts of data



Example: Scintillator Signal

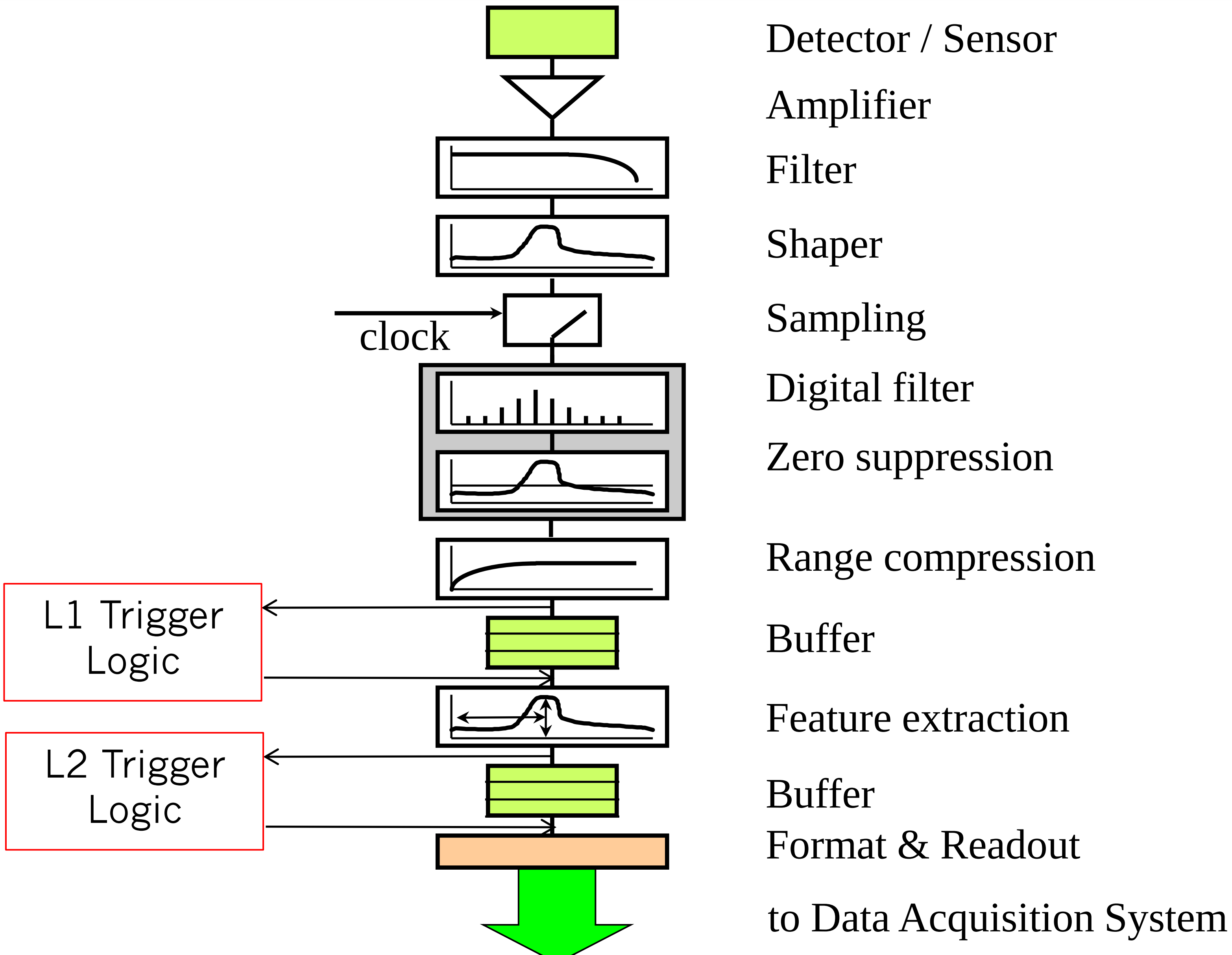
Photomultiplier serves as the amplifier

Measure if pulse height is over a threshold



from H. Spieler "Analog and Digital Electronics for Detectors"

Many Steps of Processing Before Readout!



Filtering & Shaping

Purpose is to adjust signal for the measurement desired

- Broaden a sharp pulse to reduce input bandwidth & noise
  - Make it too broad and pulses from different times mix
- Analyze a wide pulse to extract the impulse time and integral ⇒

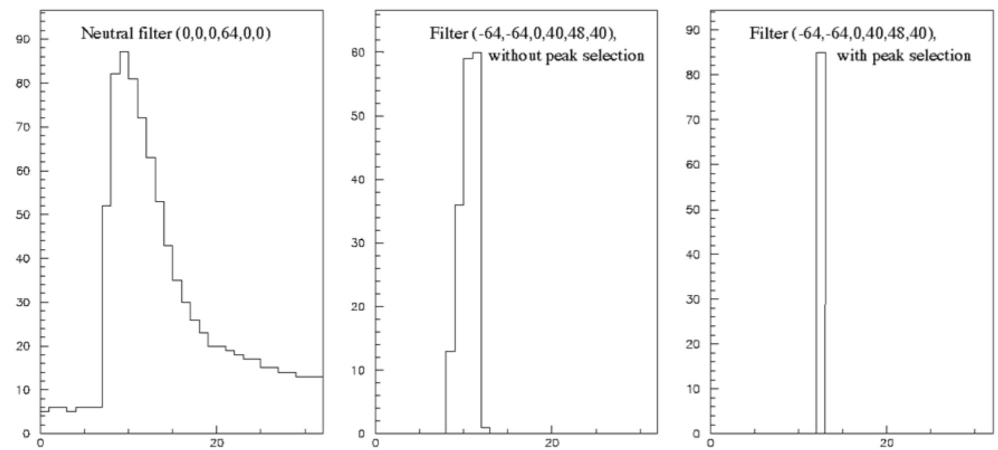
Example: Signals from scintillator every 25 ns

- Need to sum energy deposited over 150 ns
- Need to put energy in correct 25 ns time bin
- Apply digital filtering & peak finding
  - Will return to this example later

In the trigger path, **digital filtering** followed by a **peak finder** is applied to energy sums **(L1 Filter)**

Efficiency for energy sums above 1 GeV should be close to 100% (depends on electronics noise)

Pile-up effect: for a signal of 5 GeV the efficiency is close to 100% for pile-up energies up to 2 GeV (CMS)



Sampling & Digitization

Signal can be stored in analog form or digitized at regular intervals (sampled)

- Analog readout: store charge in analog buffers (e.g. capacitors) and transmit stored charge off detector for digitization
- Digital readout with analog buffer: store charge in analog buffers, digitize buffer contents and transmit digital results off detector
- Digital readout with digital buffer: digitize the sampled signal directly, store digitally and transmit digital results off detector
- Zero suppression can be applied to not transmit data containing zeros
  - Creates additional overhead to track suppressed data

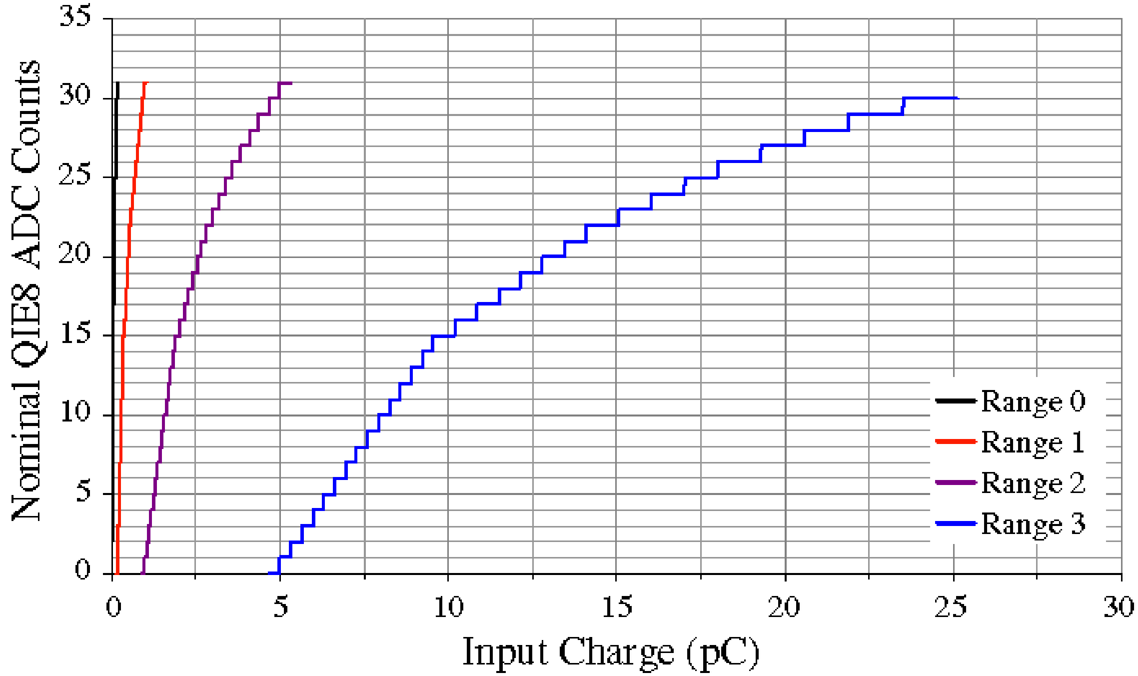
Signal can be discriminated against a threshold

- Binary readout: all that is stored is whether pulse height was over threshold

Range Compression

Rather than have a linear conversion from energy to bits, vary the number of bits per energy to match your detector resolution and use bits in the most economical manner.

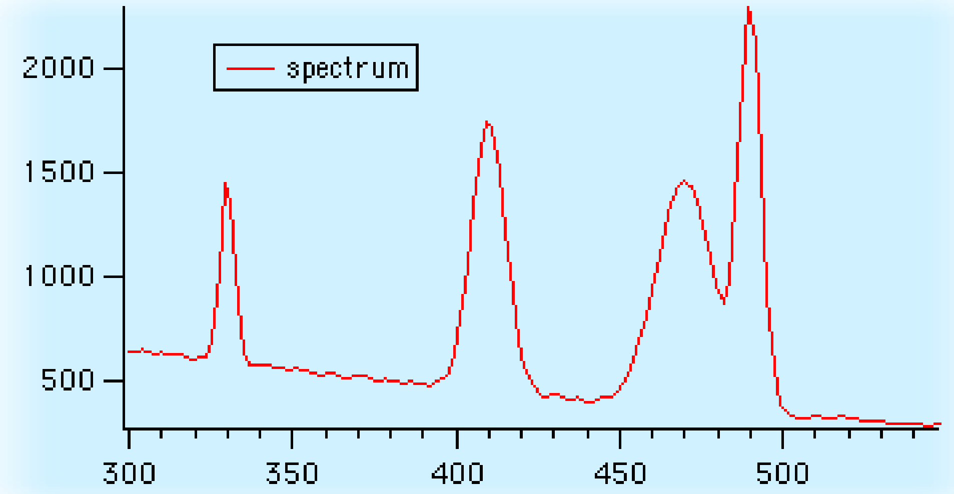
- Have different ranges with different nos. of bits per pulse height
- Use nonlinear functions to match resolution

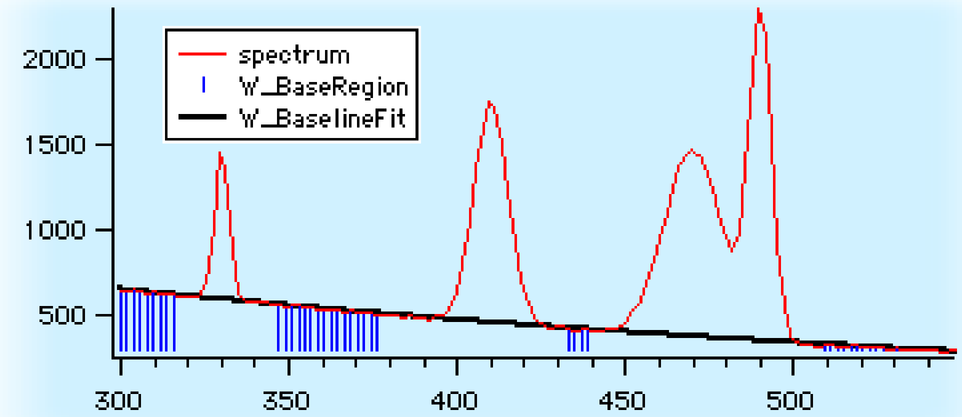


Baseline Subtraction

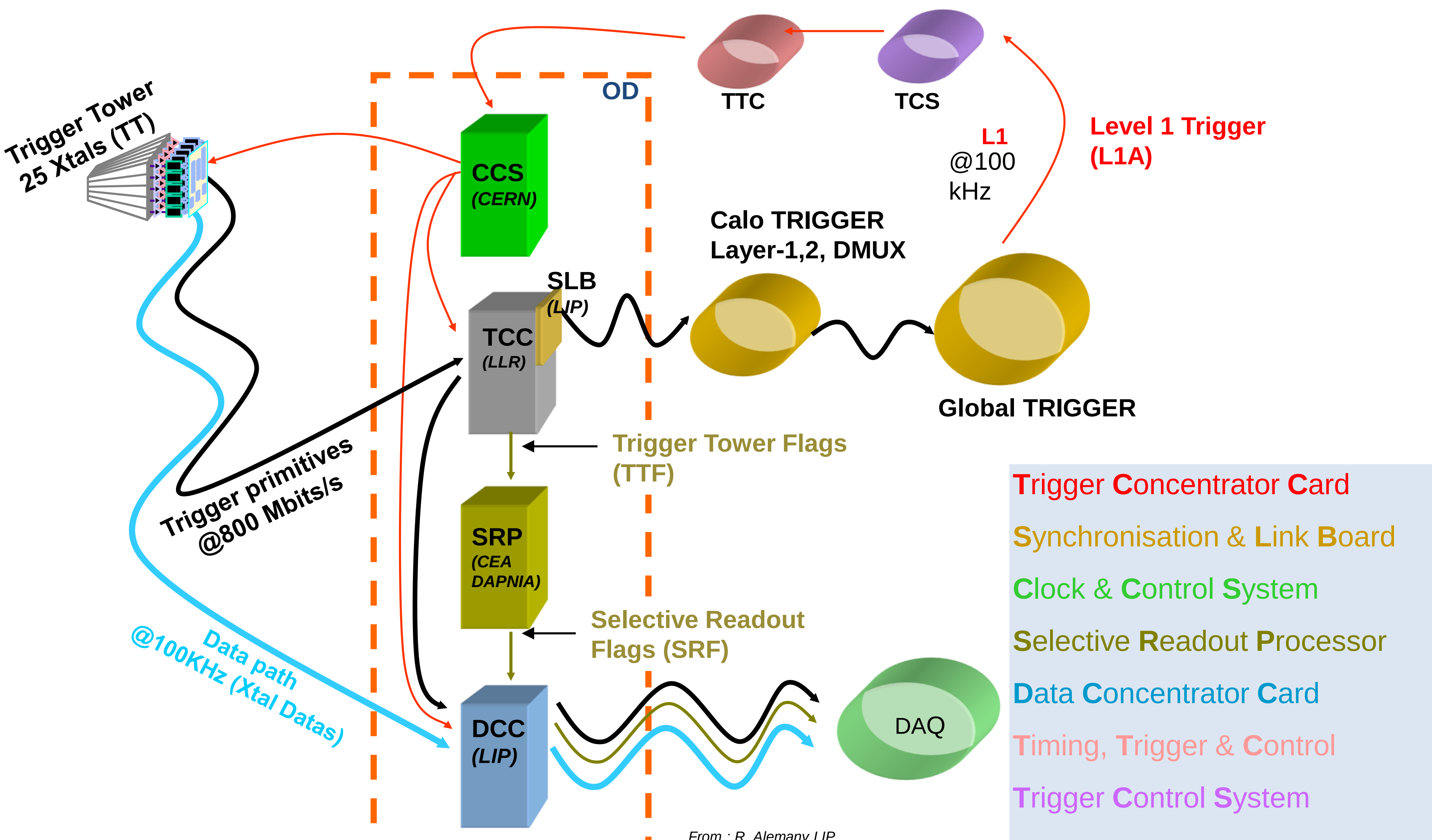
Wish to measure the integral of an individual pulse on top of another signal

- Fit slope in regions away fr
- Subtract integral under fitte





EM Calorimeter Trigger/DAQ Processing



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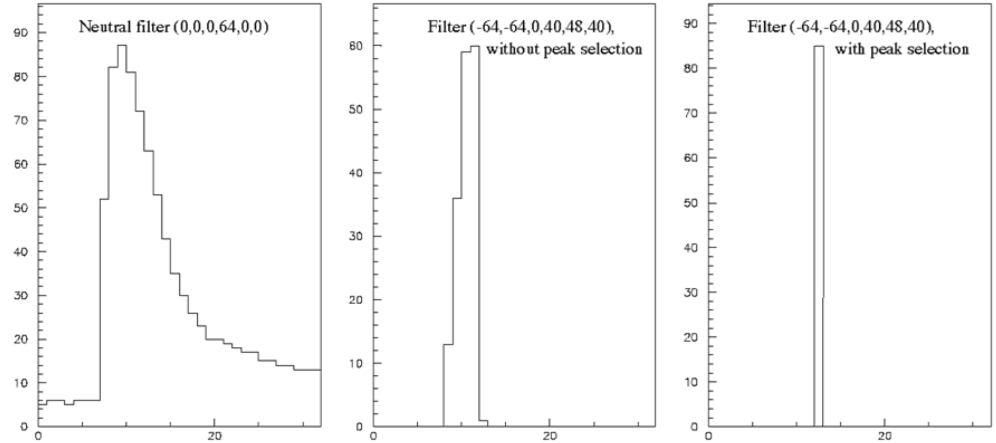
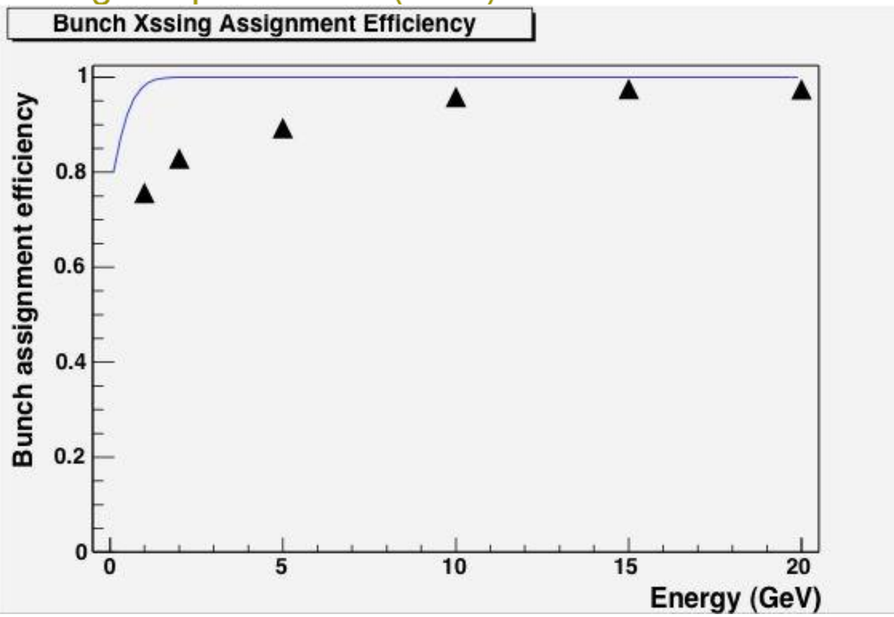
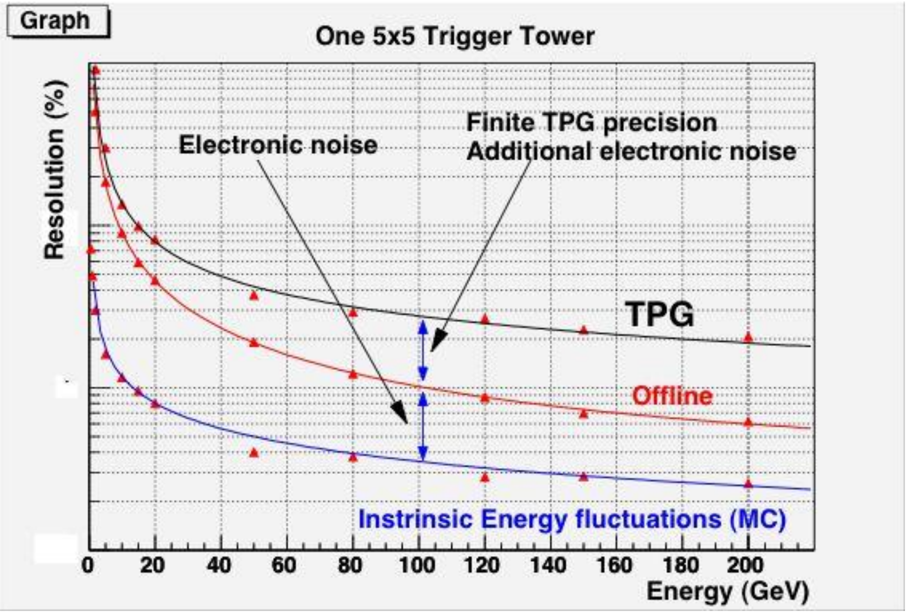
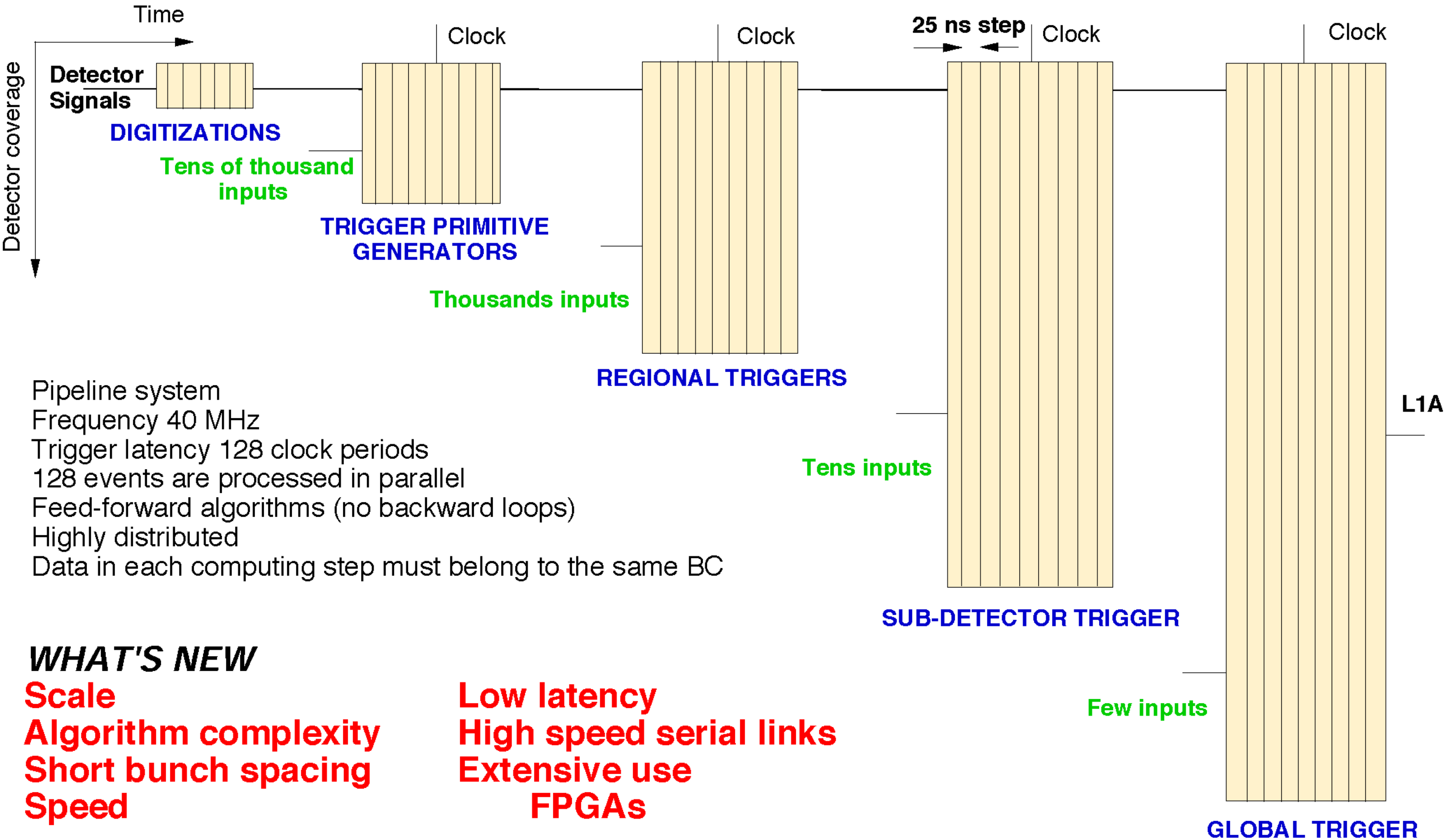


Test beam results (45 MeV per xtal):





Level 1 Trigger Organization



Pipeline system
Frequency 40 MHz
Trigger latency 128 clock periods
128 events are processed in parallel
Feed-forward algorithms (no backward loops)
Highly distributed
Data in each computing step must belong to the same BC

WHAT'S NEW

Scale
Algorithm complexity
Short bunch spacing
Speed

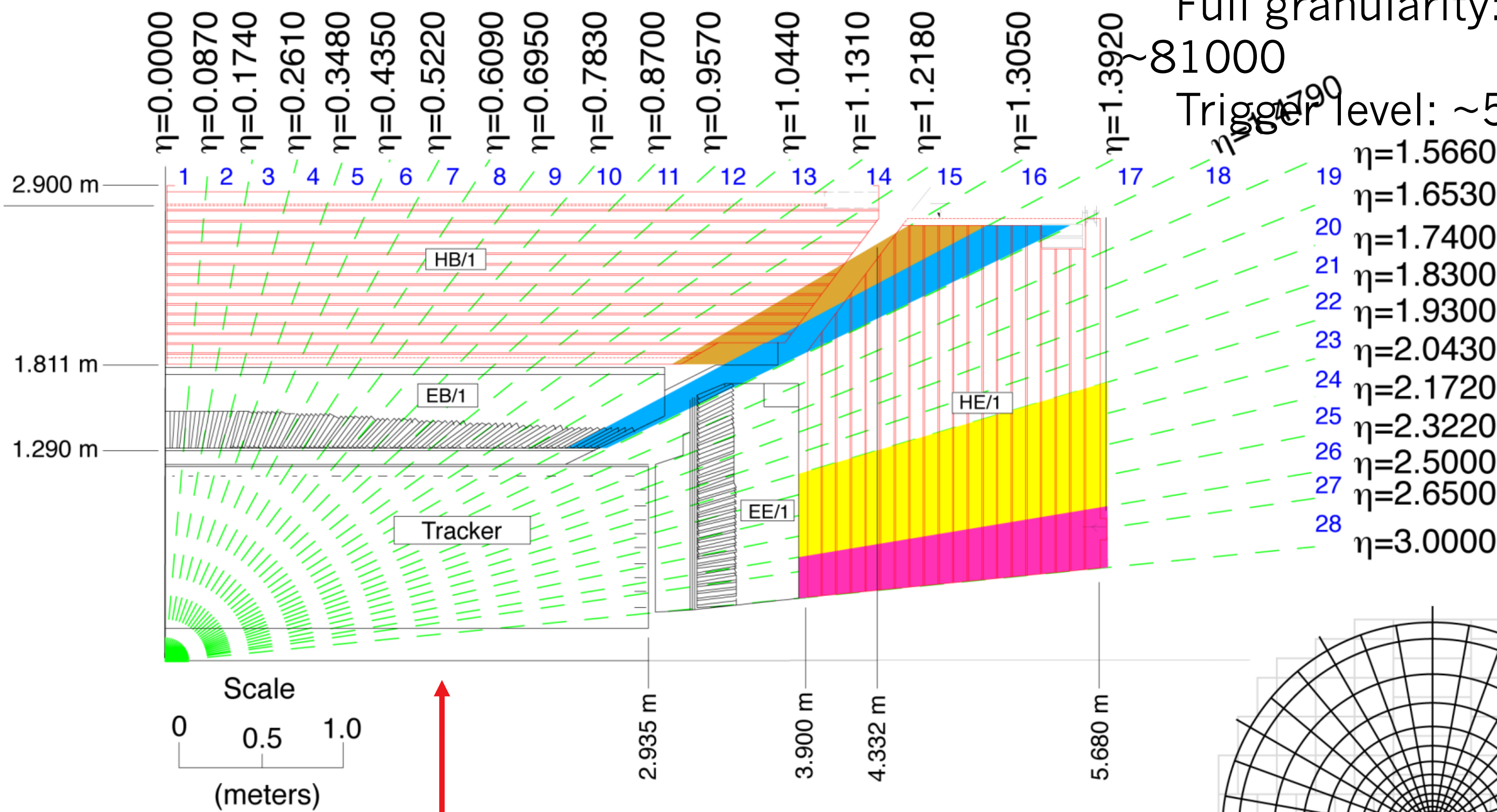
Low latency
High speed serial links
Extensive use FPGAs

CMS Calorimeter Geometry

Channel Count

Full granularity: ~81000

Trigger level: ~5000



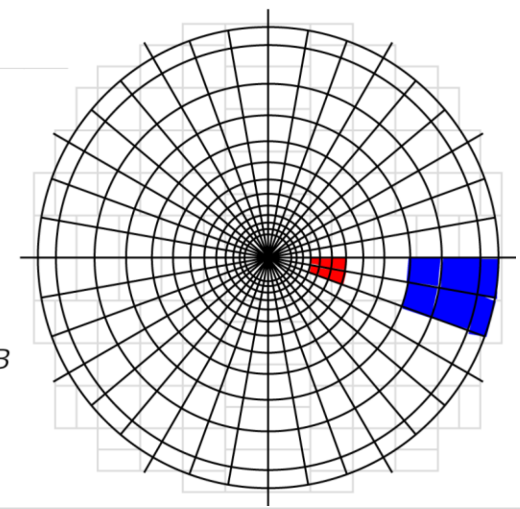
EB, EE, HB, HE map to 18 RCT crates

Provide e/γ and jet, τ, E_T triggers

2 CMS HF Calorimeters mapping onto Trigger System HF Crate

Readout segmentation: 36φ × 12η × 2z × 2F/B

Trigger Tower segmentation: 18φ × 4η × 2F/B



Channels – Channels - Channels

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Calorimeter Trigger Input from ECAL and HCAL (Phase-1)

Geometry	η-divisions	ϕ-divisions	Bits/E,H-tower ET, feature	Bandwidth (Gbps)	Fiber Count 4.8 – 6.4 Gbps
Barrel +/-	17+17	72	8+1+8+6	2252	324 + 306
Endcap +/-	11+11	72	8+1+8+6	1457	198 + 198
Total	56	72	23	3609	1026

18 cards, 1 FPGA/card, ~56 4.8-6.4-Gbps inputs per card

Barrel Calorimeter Trigger Input ECAL & HCAL (Phase-2)

Geometry	η-divisions	ϕ-divisions	Bits/E-crystal Bits/H-tower	Bandwidth (Gbps)	Fiber Count 16 Gbps
ECAL Crystals	17x5	72x5	10	208080	3060
HCAL Towers	16	72	8+6	645	144
Total	-	-	-	208745	3204

24 cards, 1 FPGA/card, 106 25-Gbps inputs per card

Technologies of Choice → LHC Schedules

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FPGA & Telecom technology advances (VME → μTCA → ATCA)

- Ubiquitous >10 Gbps links
- FPGAs with O(100) rx/tx links with built in serdes
  - Xilinx Kintex / Virtex-7 → Ultrascale platforms
  - Gigantic cores
  - DSP units, BRAM and Embedded processors (ZYNQ)
- Fiber optic components
  - Avago mini-pods at 10 Gbps → Samtec Firefly 25 Gbps capable units

LHC long shutdown 1: 2013-2014 (Phase-1 Upgrades)

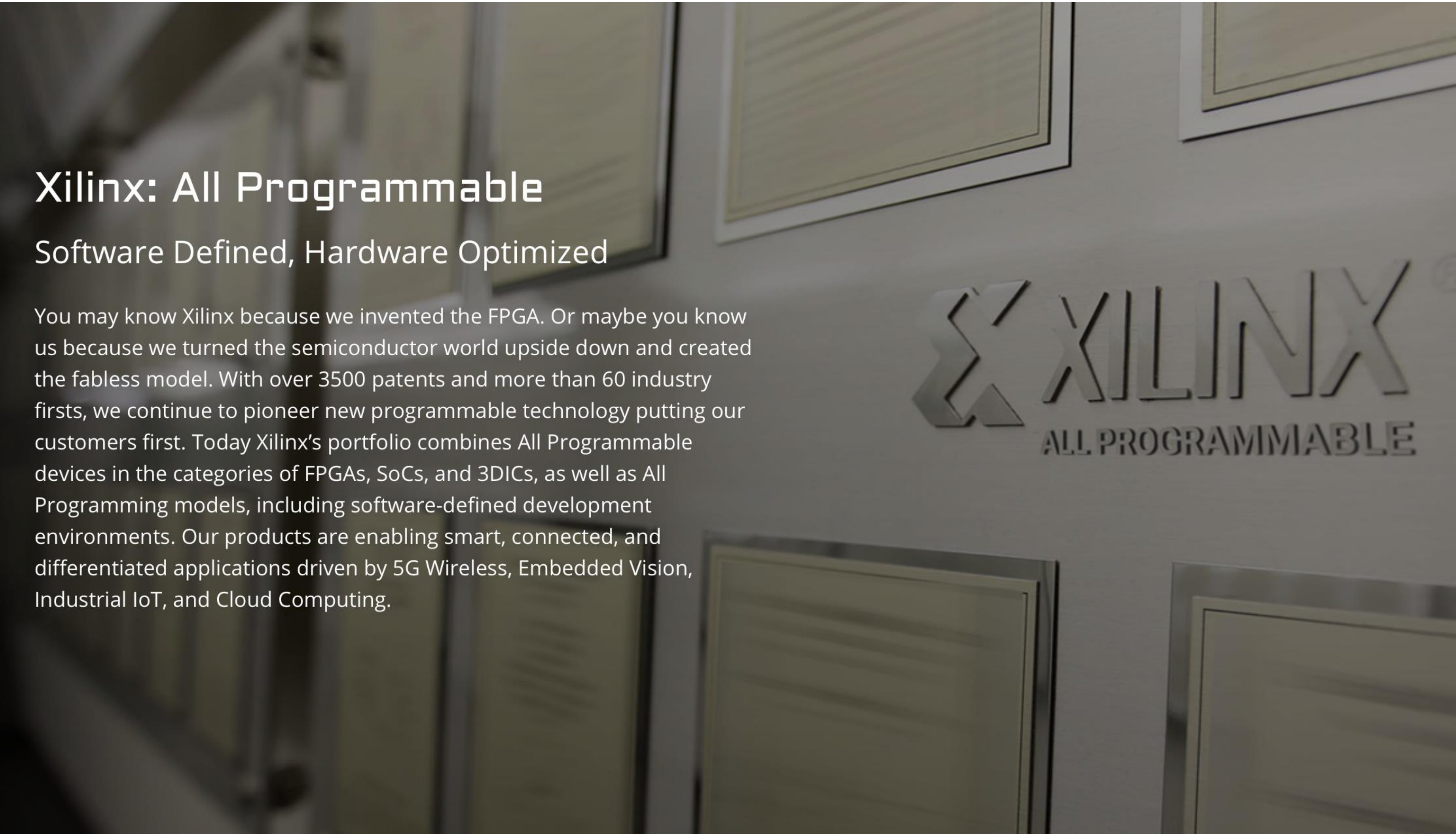
- Virtex-7 family cards
  - In CMS: CTP7 (Wisconsin), MP7 (Imperial), MTF7 (Florida)
- 10 Gbps optics

LHC long shutdown 3: 2026-2027 (Phase-2 Upgrades)

- Ultrascale family
  - In CMS: APx (Wisconsin), Serenity (Imperial), X2O (UCLA), Apollo (Cornell)
- 25 Gbps optics

Similar capability boards in ATLAS as well

Xilinx Field Programmable Gate Arrays



FPGA Slice

Array of well-defined logic cells, driven by LUTs

Software configured connections

Cleverly organized

Preconfigured digital logic elements

Arranged in a rectangular grid for efficient parallel processing

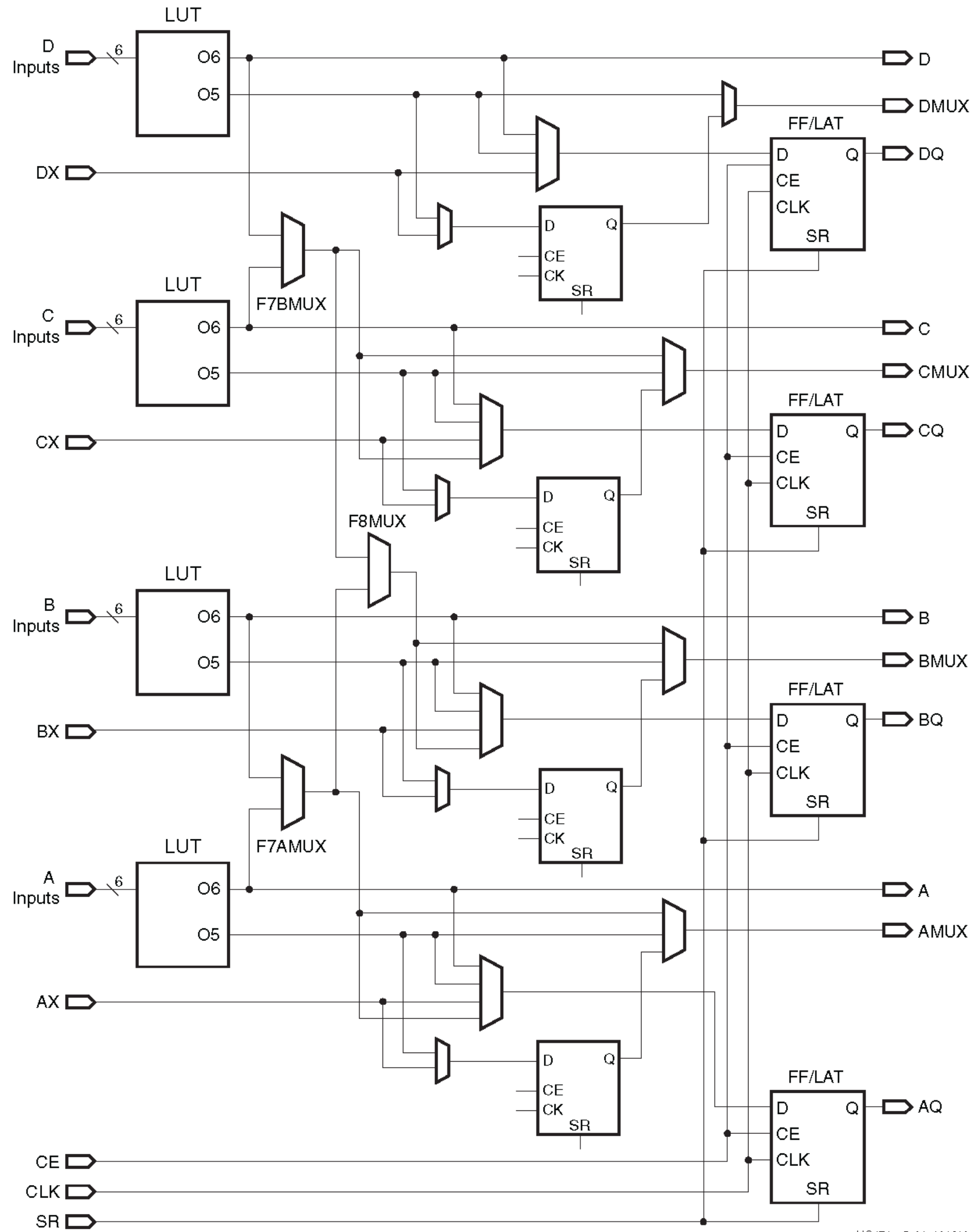


Figure 5-1: **Simplified 7 Series FPGA Slice**

Configurable Logic Block

Firmware developer uses programming languages to define “connections”

Firmware tools create the “bit file” which defines the switch matrix / LUTs

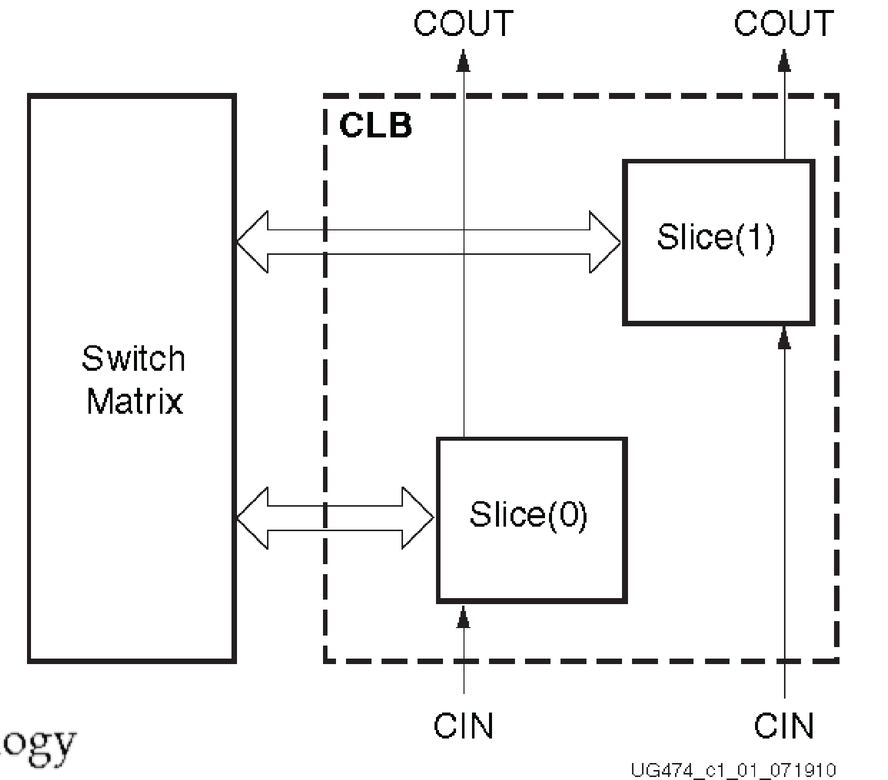


Figure 1-1: **Arrangement of Slices within the CLB**

- Real 6-input look-up table (LUT) technology
- Dual LUT5 (5-input LUT) option
- Distributed Memory and Shift Register Logic capability
- Dedicated high-speed carry logic for arithmetic functions
- Wide multiplexers for efficient utilization

CLBs are the main logic resources for implementing sequential as well as combinatorial circuits. Each CLB element is connected to a switch matrix for access to the general routing

Abundant Logic Resources in Virtex-7 Family

Table 1-4: **Virtex-7 FPGA CLB Resources**

Device	Slices[1]	SLICEL	SLICEM	6-input LUTs	Distributed RAM (Kb)	Shift Register (Kb)	Flip-Flops
7V585T	91,050	63,300	27,750	364,200	6,938	3,469	728,400
7V2000T	305,400	219,200	86,200	1,221,600	21,550	10,775	2,443,200
7VX330T	51,000	33,450	17,550	204,000	4,388	2,194	408,000
7VX415T	64,400	38,300	26,100	257,600	6,525	3,263	515,200
7VX485T	75,900	43,200	32,700	303,600	8,175	4,088	607,200
7VX550T	86,600[2]	51,700	34,900	346,400	8,725	4,363	692,800
7VX690T	108,300	64,750	43,550	433,200	10,888	5,444	866,400
7VX980T	153,000	97,650	55,350	612,000	13,838	6,919	1,224,000
7VX1140T	178,000	107,200	70,800	712,000	17,700	8,850	1,424,000
7VH580T	90,700	55,300	35,400	362,800	8,850	4,425	725,600
7VH870T	136,900	83,750	53,150	547,600	13,275	6,638	1,095,200

Scaling: Modular Blocks of Resources

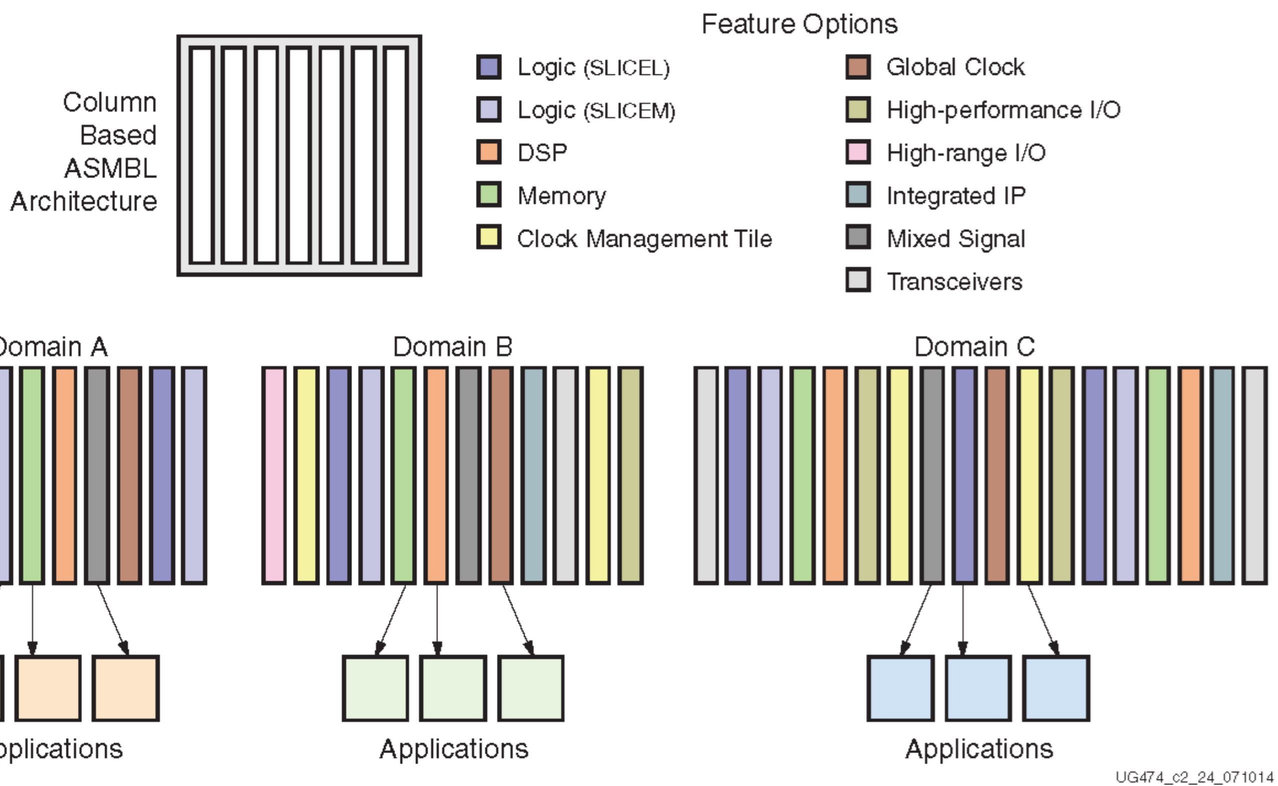


Figure 2-1: **ASMBL Architecture**

The ASMBL architecture breaks through traditional design barriers by:

- Eliminating geometric layout constraints such as dependencies between I/O count and array size.
- Enhancing on-chip power and ground distribution by allowing power and ground to be placed anywhere on the chip.
- Allowing disparate integrated IP blocks to be scaled independent of each other and surrounding resources.

Xilinx FPGAs – Phase-1 Choice: V7 690T

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Xilinx Multi-Node Product Portfolio Offering

45nm	28nm	20nm	16nm
SPARTAN 6	VIRTEX 7 KINTEX 7	VIRTEX UltraSCALE KINTEX UltraSCALE	VIRTEX UltraSCALE+ KINTEX UltraSCALE+

Cost-Optimized Portfolio

Spartan-7	Spartan-6
Artix-7	Zynq-7000

7 Series

Spartan-7	Artix-7
Kintex-7	Virtex-7

UltraScale

Kintex UltraScale	Virtex UltraScale

UltraScale+

Kintex UltraScale+	Virtex UltraScale+

	Spartan-7	Artix-7	Kintex-7	Virtex-7
Max Logic Cells (K)	102	215	478	1,955
Max Memory (Mb)	4.2	13	34	68
Max DSP Slices	160	740	1,920	3,600
Max Transceiver Speed (Gb/s)	--	6.6	12.5	28.05
Max I/O Pins	400	500	500	1,200

Key element - Multi-gigabit Opto-electronics

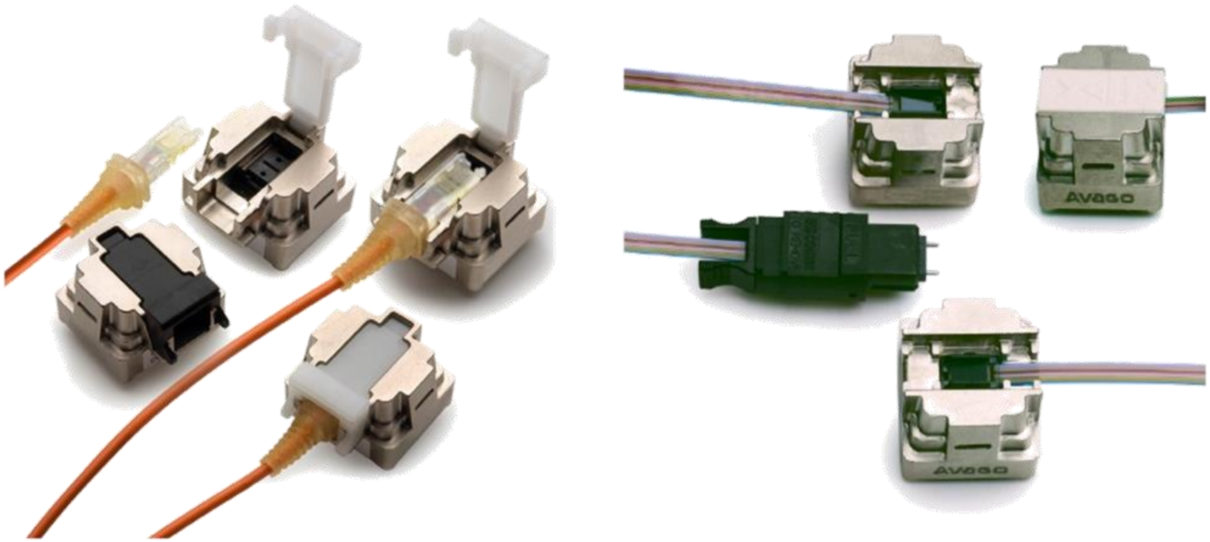


Figure 1. MiniPOD™ Transmitter and Receiver Modules with a) Round Cable and b) Flat Cable: shown with and without dust covers (White = Tx, Black = Rx).

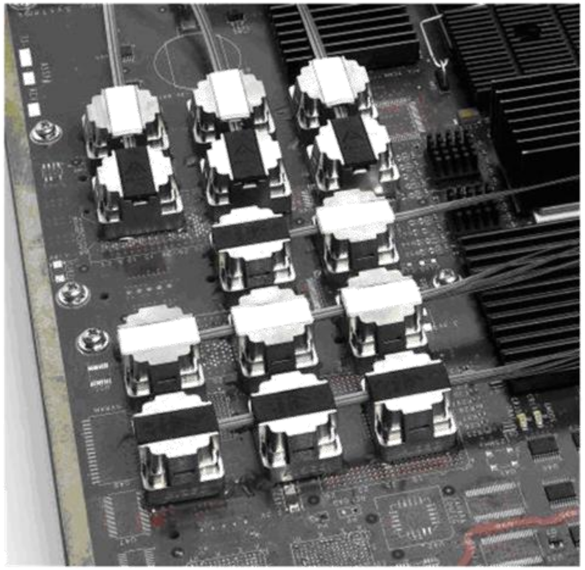


Figure 2. MiniPOD™ Transmitter and Receiver flat ribbon cable modules in a tiled arrangement example.

Key Product Parameters

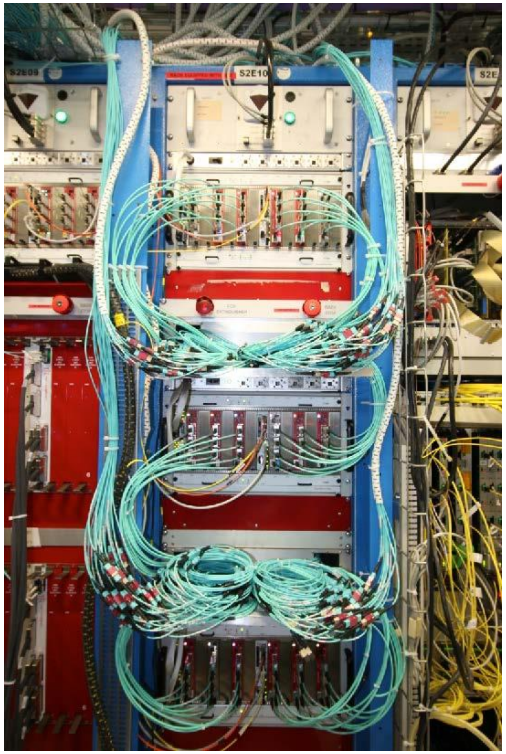
The Avago Technologies MiniPOD™ modules operate at 850 nm and are compliant to the Multi-mode Fiber optical specs in clause 86 and relevant electrical specs in annex 86A of the IEEE 802.3ba specifications.

Parameter	Value	Units	Notes
Data rate per lane	10.3125	Gbps	As per 802.3ba: 100GBASE-SR10 and nPPI specifications
Number of operational lanes	12		100GbE operation utilizes the middle ten lanes (Rx and Tx) of the 12 physically defined lanes
Link Length	100 150	m m	OM3, 2000 MHzMHz•km 50 µm MMF OM4, 4700 MHz•km 50 µm MMF

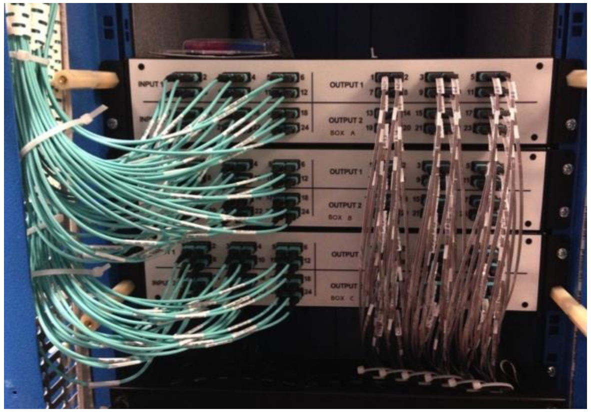
CMS Calorimeter Trigger Run-2

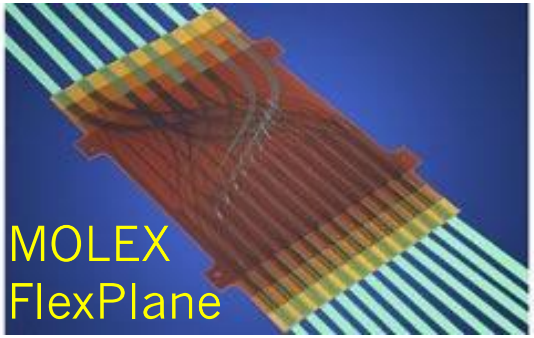
- Installed and commissioned in 2015, fully operational in 2016
  - Connections to CTP7 from Layer-1 patch panels completed in 2015
  - Connections from Layer-1 to Layer-2 via compact patch panel
    - 3 “pizza box” sized patch panels instead of full 56U rack with LC connectors
  - Layer 2 to demux to new μGT connected

Layer-1 CTP7

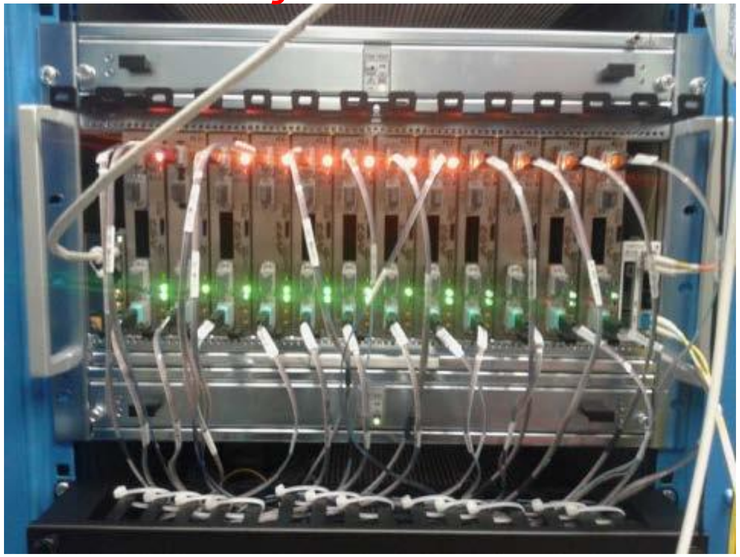


Layer-1 to Layer-2 Patch Panel

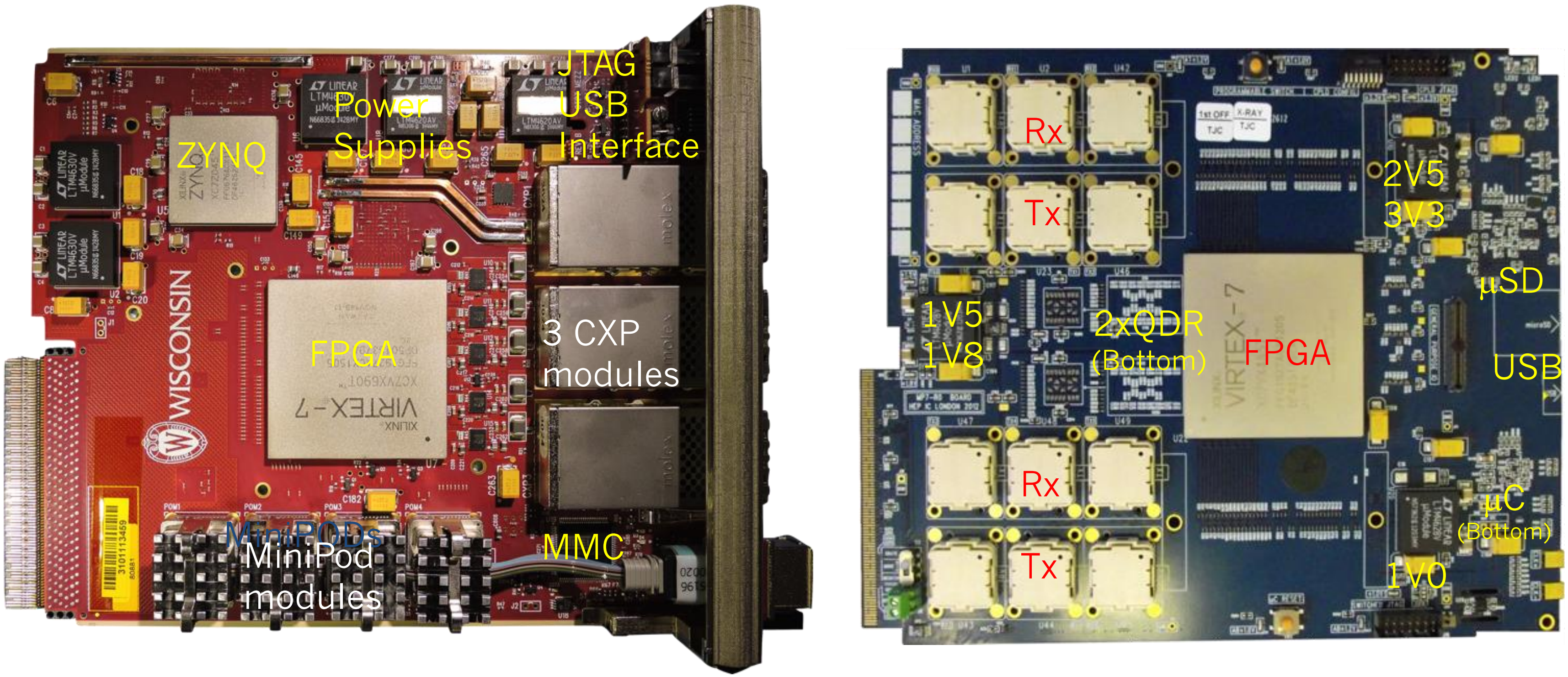




Layer-2 MP7



Level-1 Calorimeter Trigger Electronics

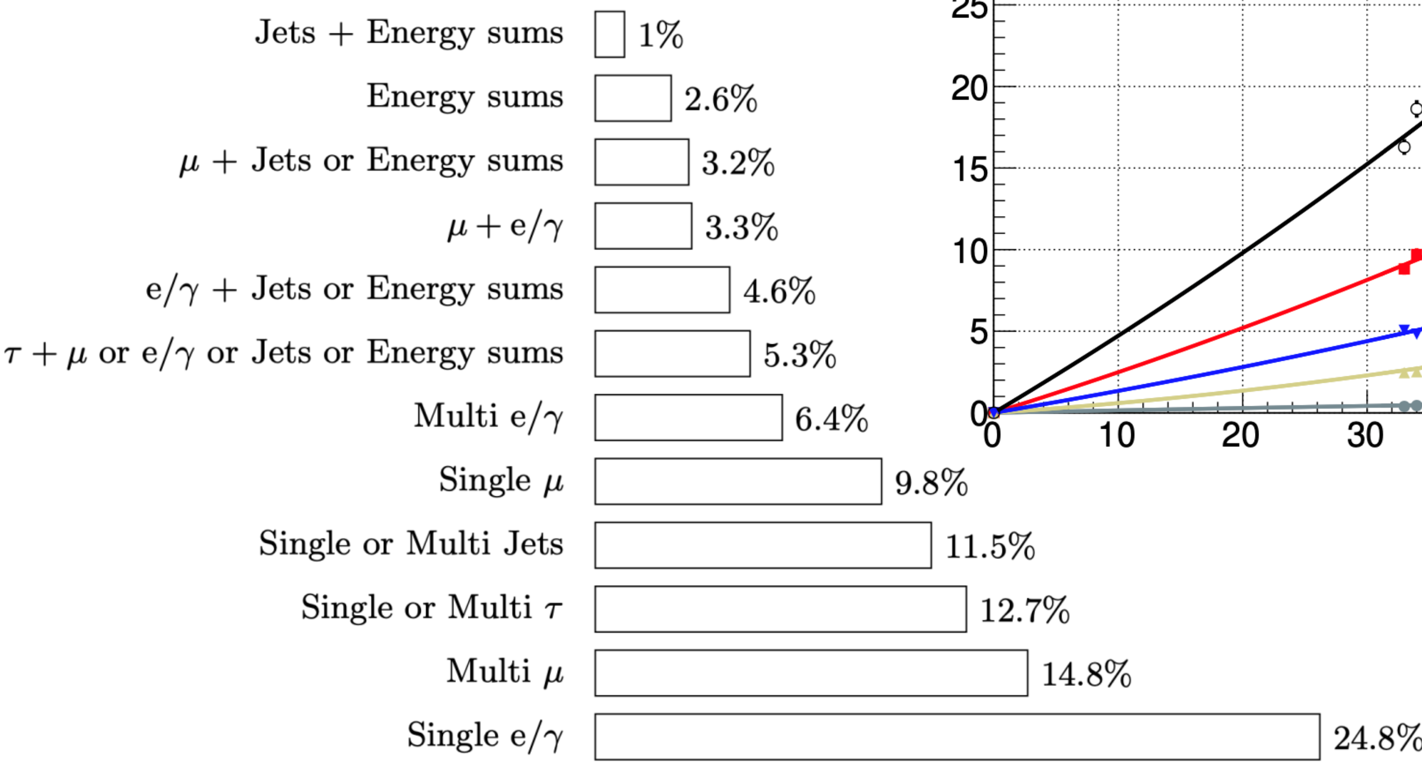


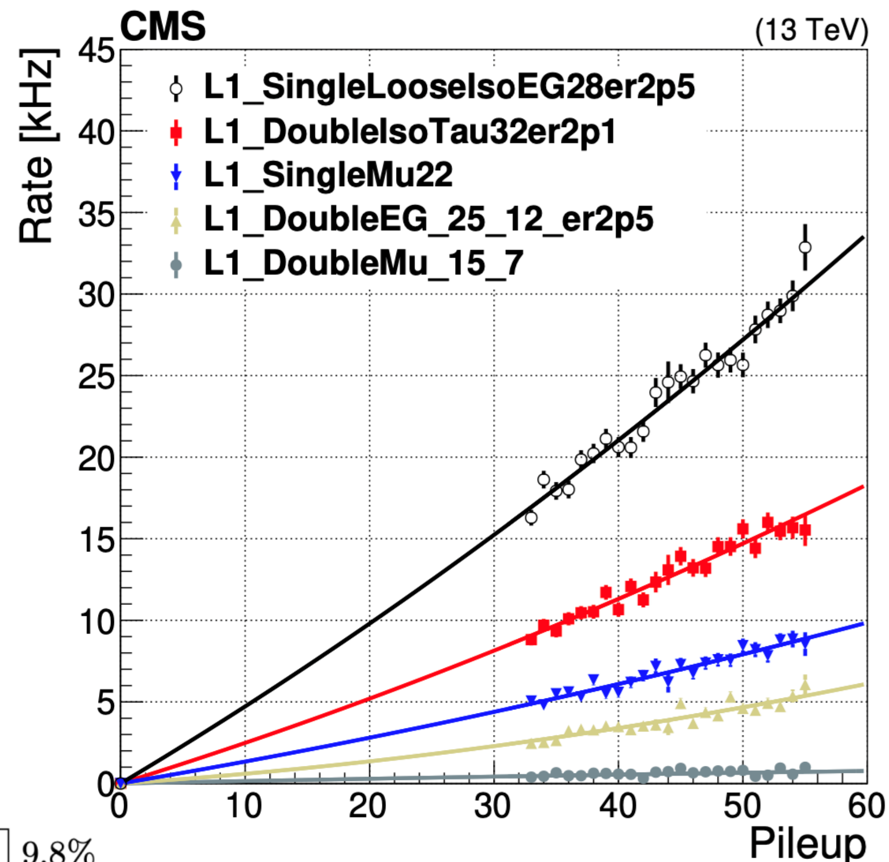
Calorimeter Trigger Processor(CTP7 – left), and Master Processor (MP7 - right)

- CTP7 (Layer-1) – µTCA Single Virtex 7 FPGA, 67 optical inputs, 48 outputs, 12 RX/TX backplane
  - Virtex 7 allows 10 Gb/s link speed on 3 CXP(36 TX & 36 RX) and 4 MiniPODs (31 RX & 12 TX)
  - ZYNQ processor running Xilinx PetaLinux for service tasks, including virtual JTAG cable
- MP7 (Layer-2) – µTCA Single Virtex 7 FPGA, up to 72 input & output links
  - Virtex 7 has 72 input and output links at 10 Gb/s
  - Dual 72 or 144MB QDR RAM clocked at 500 MHz

L1 Trigger Summary from Run-2,3

We capture the physics of interest within 100 kHz bandwidth, while discarding majority of 32 kHz of collisions





CICADA – Machine Learning in L1T

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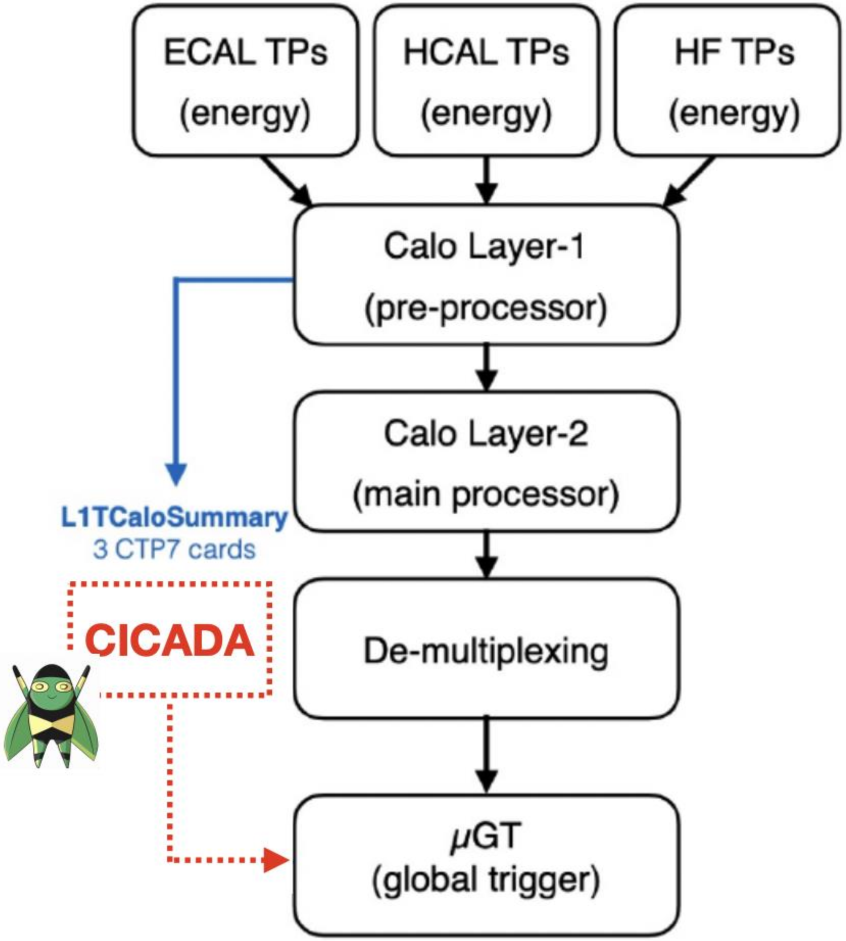
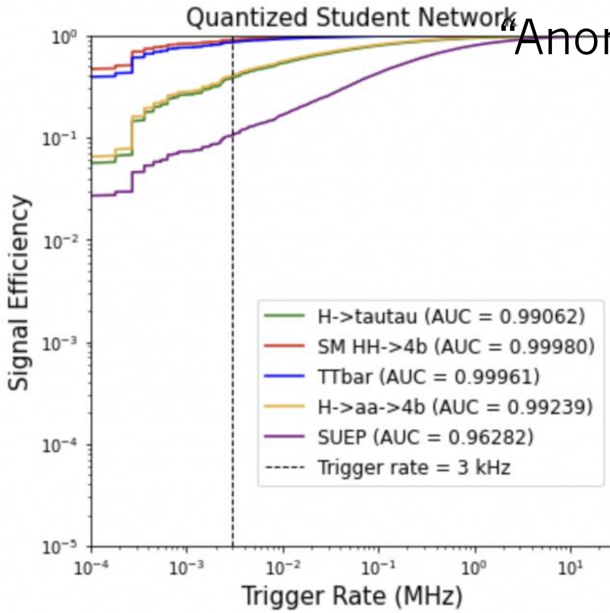
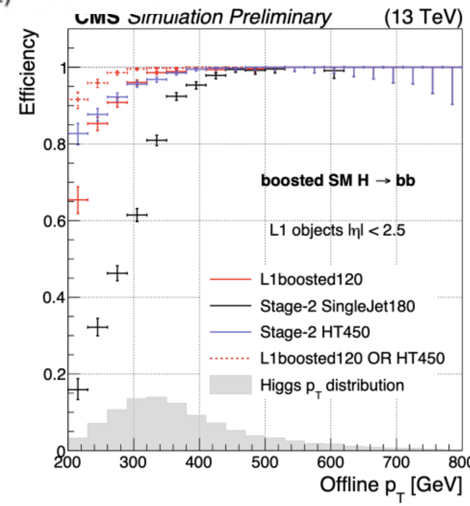


Unsupervised learning
"Anomaly Detection"
Ho-Fung Tsoi



Also includes new (but traditional) boosted object algorithm
Pallabi Das



LHC Now → HL-LHC in the Future

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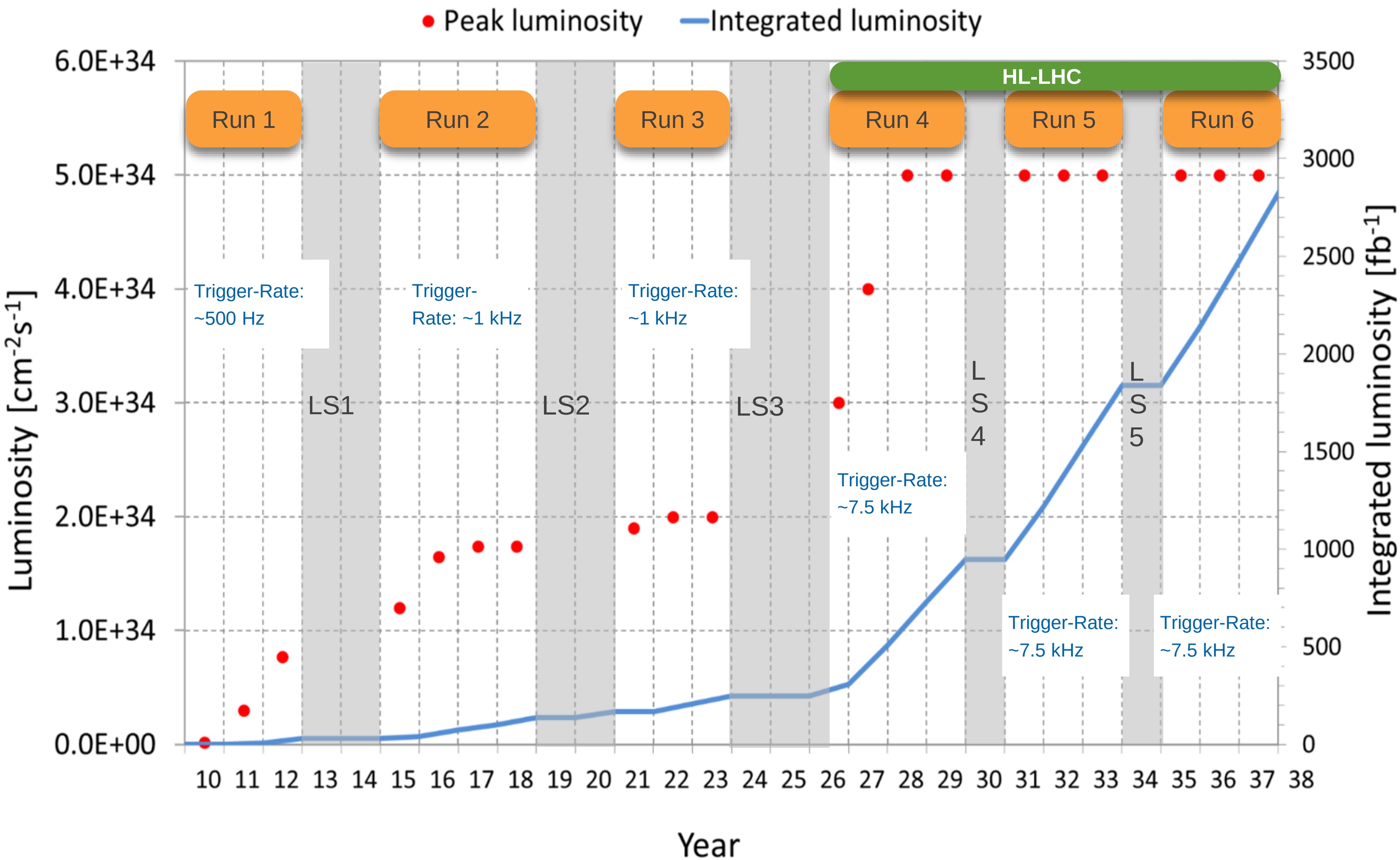


CMS will be on path to exabytes of data acquired in the HL-LHC era

HLLHC Parameters

Parameter	Nominal LHC Design Report	HL-LHC 25 ns standard	HL-LHC 25 ns BCMS	HL-LHC 8b4e
Beam energy in collision [TeV]	7	7	7	7
$N_b [10^{11}]$	1.15	2.2	2.2	2.3
Number of bunches per beam	2808	2748	2604	1968
Beam current [A]	0.58	1.09	1.03	0.82
Minimum β^* [m]	0.55	0.2	0.2	0.2
ϵ_n [μm]	3.75	2.50	2.50	2.20
ϵ_L [eVs]	2.50	2.50	2.50	2.50
Peak luminosity with crab cavities $[10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}]$	(1.18) Operating at 2x now	12.6	11.9	11.6
Levelled luminosity for $\mu = 140[10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}]$	-	5.32	5.02	5.03
(inelastic) collisions/crossing μ (with levelling and crab cavities)	27	140	140	140
Maximum line density of pileup events during fill [events/mm]	0.21	1.3	1.3	1.3

Expect Operating at 7.5x ultimately

HLLHC Physics & Event Rates

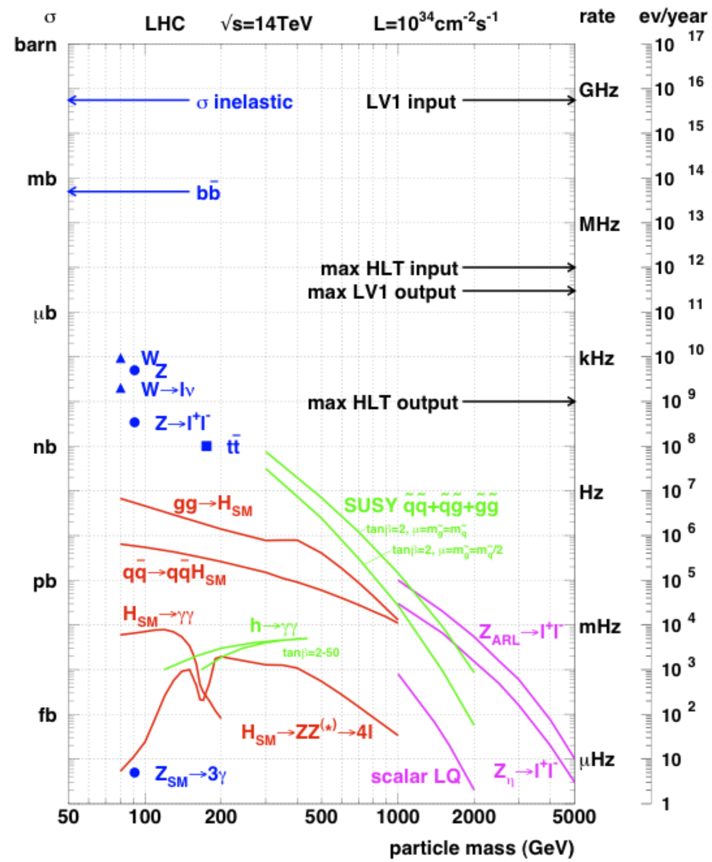
At L = 7.5 x 10^{34} cm^{-2} s^{-1}

- 200 events per beam crossing (BX)
  - ~ 7.5 GHz pp collision rate
  - "Interesting" events contain ~ 200 pileup events
- EWK rate: 7.5 kHz W & Z
- Top rate: 75 Hz
- Higgs: 1 Hz, H_{4l}: 10^{-4} Hz

Select in stages

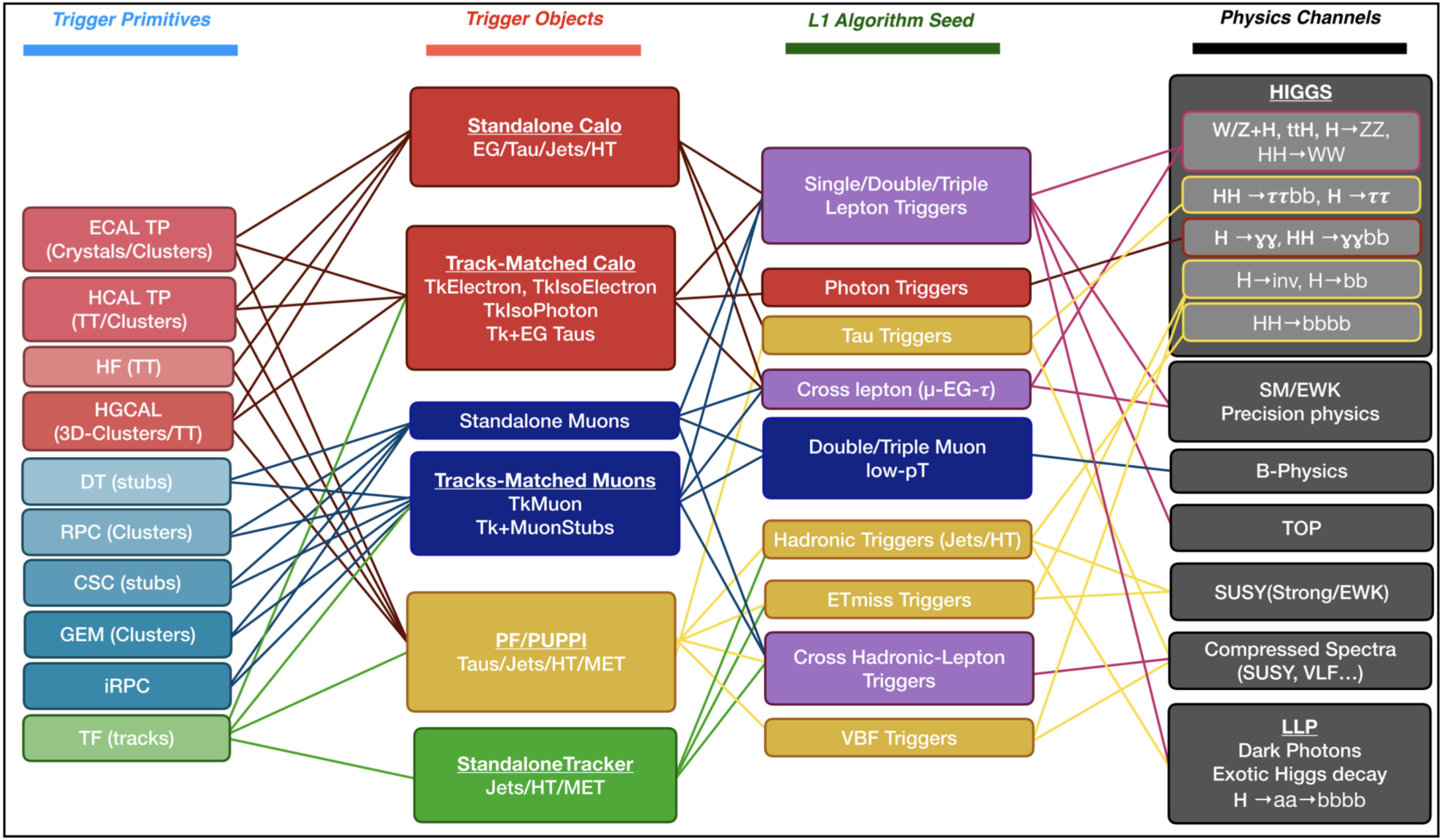
- Level-1 Triggers
  - 7.5 GHz (32 MHz BX) to 750 kHz
- High Level Triggers
  - 750 kHz to ~10 kHz

Event store: ~10 kHz events

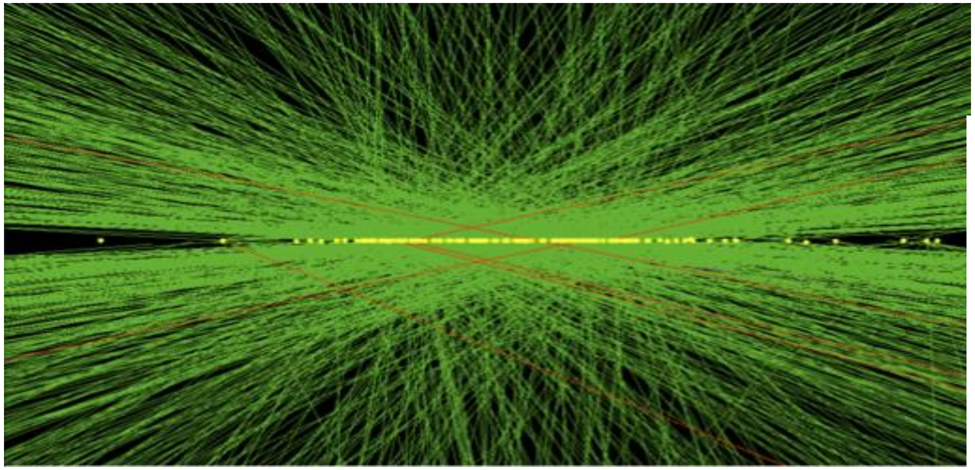


Scale shifts up by 7.5x

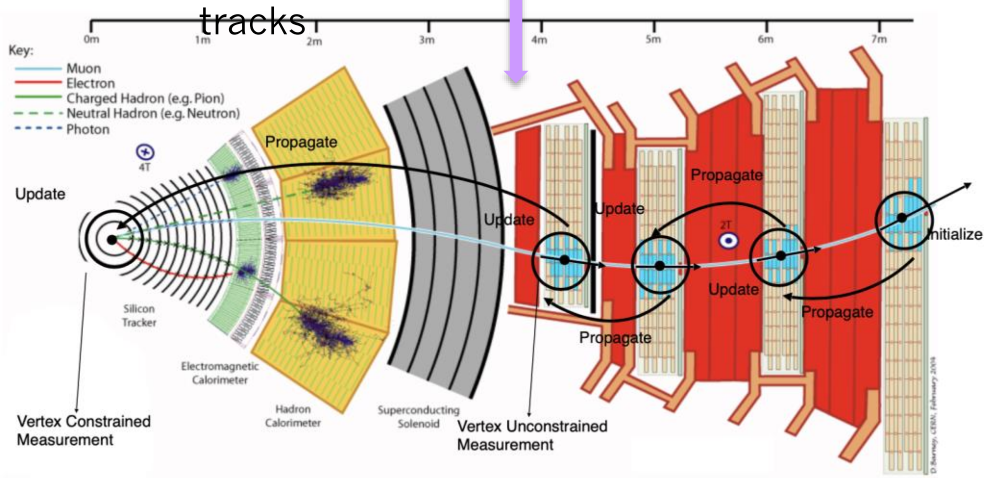
Triggers → Physics

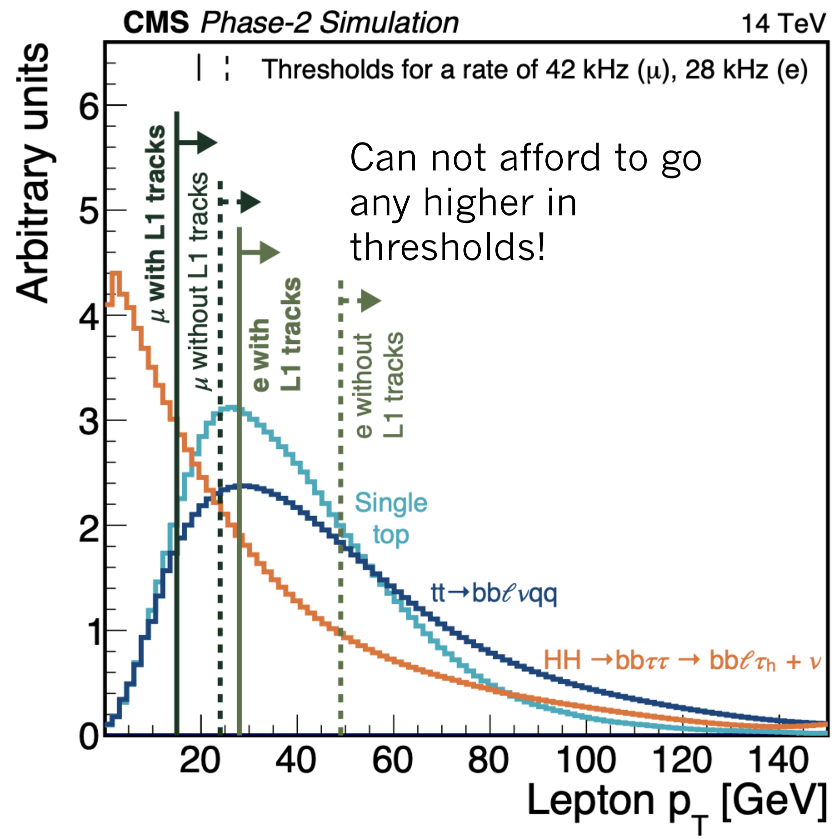


Collisions (p-p) at HLLHC



Selecting high P_T clusters and tracks





Can not afford to go any higher in thresholds!

Requirements (my slide from Feb 2004)

Calorimeter Trigger for Super LHC

Electrons, Photons, τ-jets, Jets, Missing E_T

- **Current Algorithms**
- **What can be improved?**

Bottom line

- **Must hold the thresholds low to study electro-weak symmetry breaking physics**

Only option is to further reduce the backgrounds

- **Electrons/photons/τ-jets**
  - Dominated by tails of jet fragmentation to π^0
  - Use of tracking in level-1
    - **Pixel only or pixel + outer tracker layers?**
  - Mandates higher granularity calorimeter trigger output
- **Jets and missing E_T**
  - These are real - Only minor improvement in resolution likely
  - Topology with vertex identification to reject pileup
    - **Pixel tracker provides vertex?**

Track trigger !

Crystal readout !!

S. Dasu, University of Wisconsin

February 2004 - 1

Planning ahead
(my slide from July 2005)

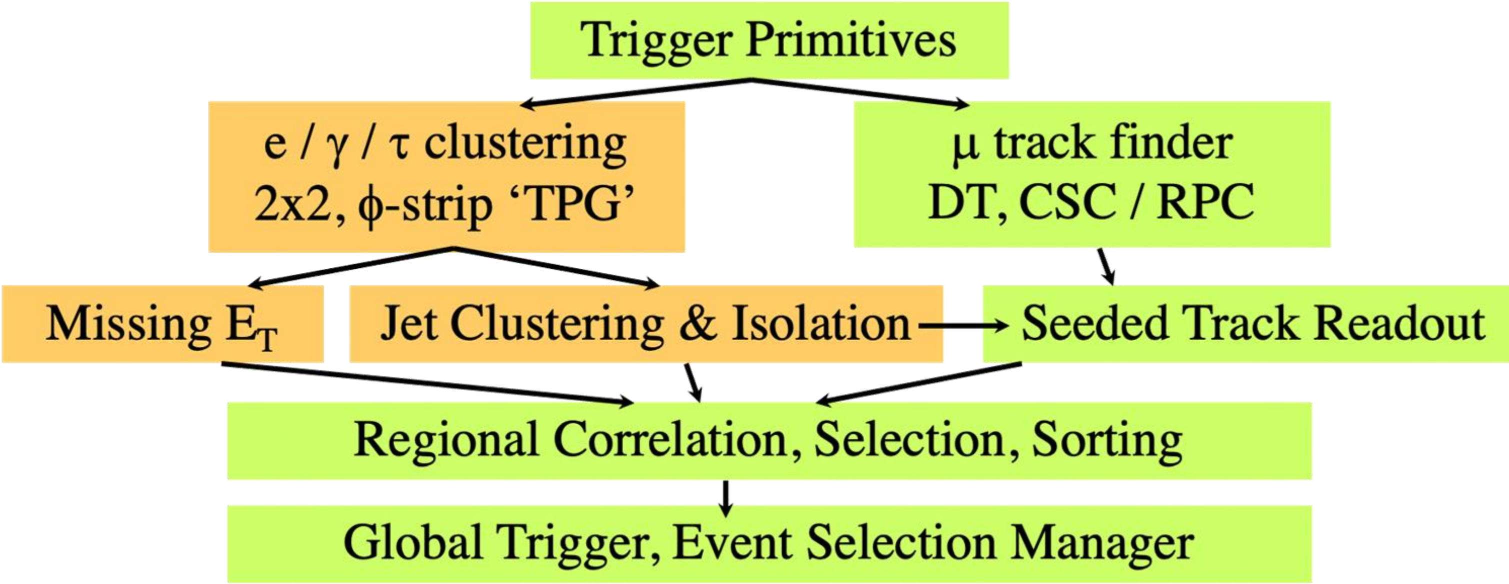
Algorithm Stages

Current:

TPG ⇒ RCT ⇒ GCT ⇒ GT

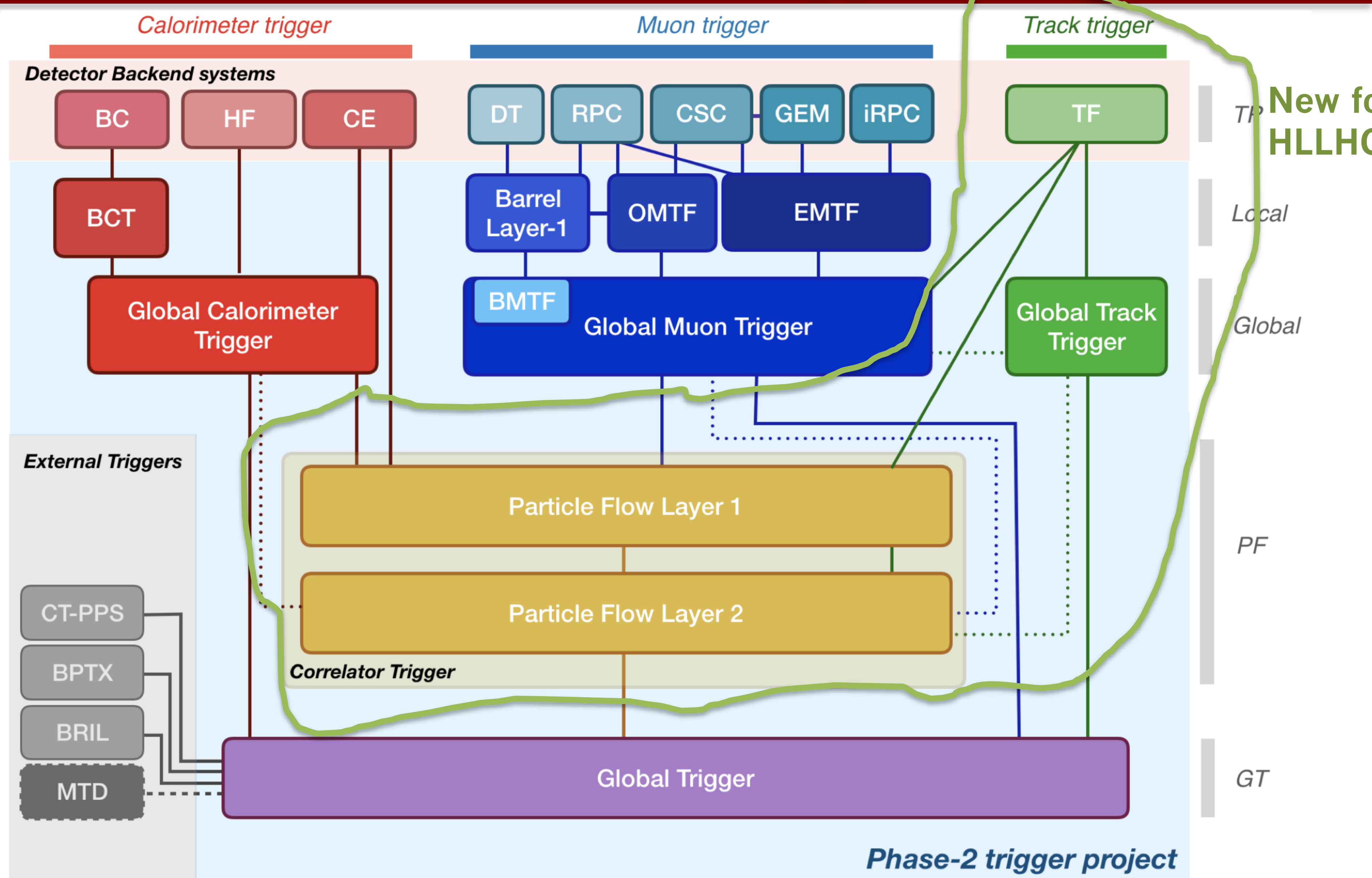
Proposed:

TPG ⇒ Clustering ⇒ Correlator ⇒ Selector



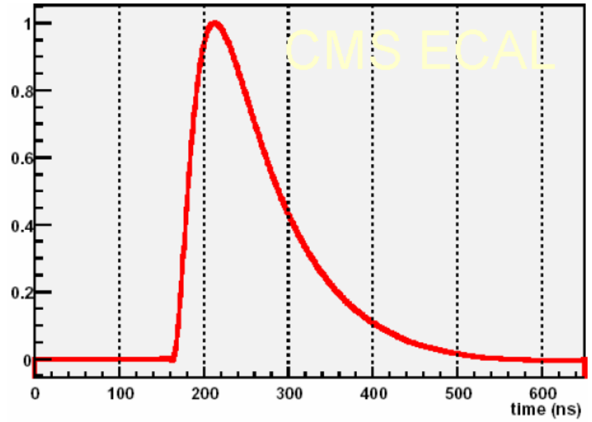
S. Dasu, University of Wisconsin — July 2005 - 5

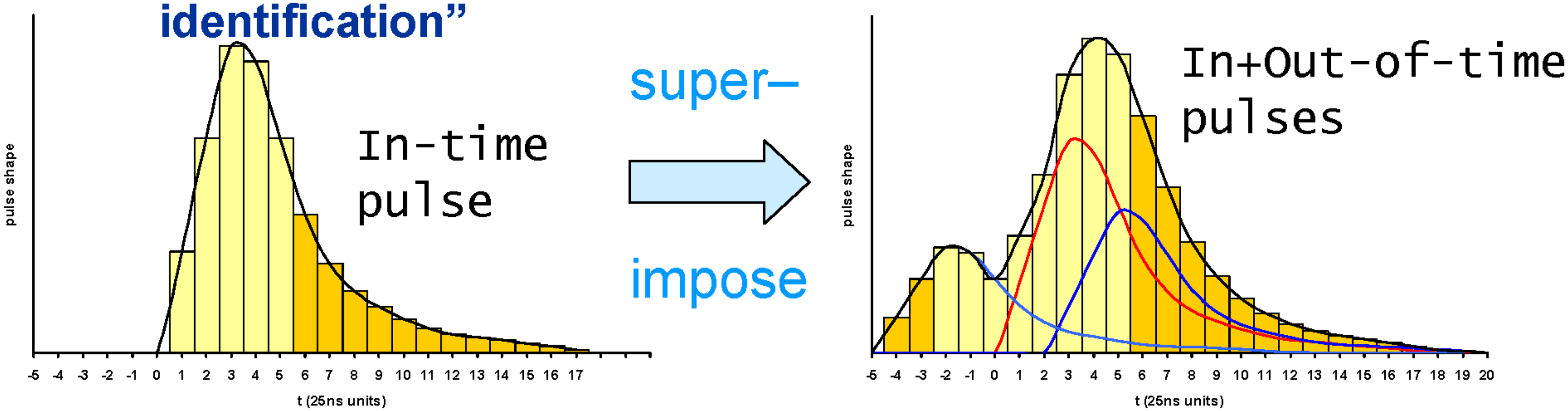
CMS HLLHC Level-1 Trigger 2020



- "In-time" pile-up: particles from the same crossing but from a different pp interaction

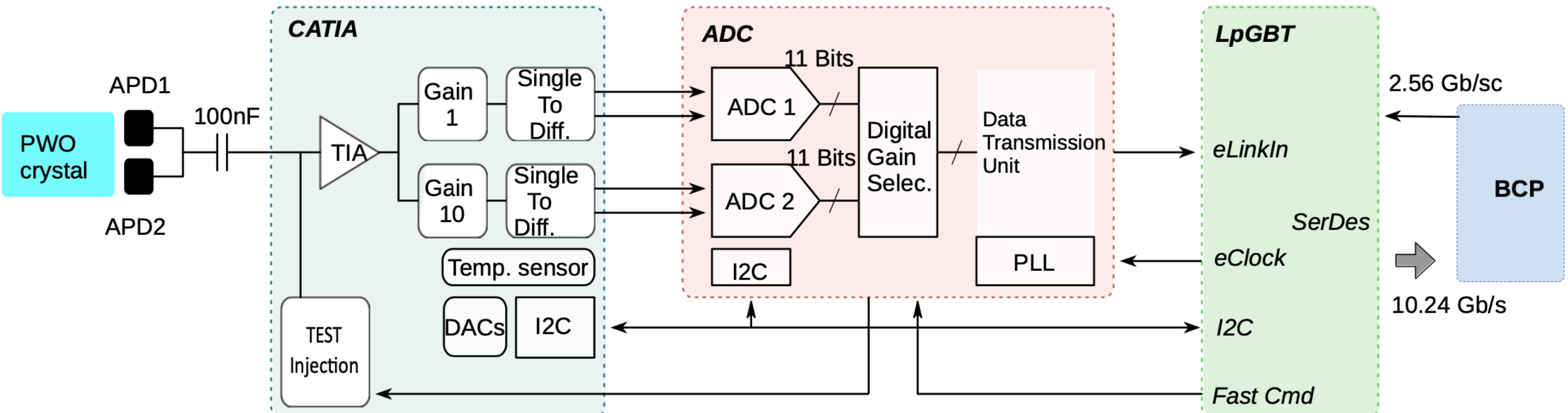
- Long detector response/pulse shapes:
  - "Out-of-time" pile-up: left-over signals from interactions in previous crossings
  - Need "bunch-crossing identification"





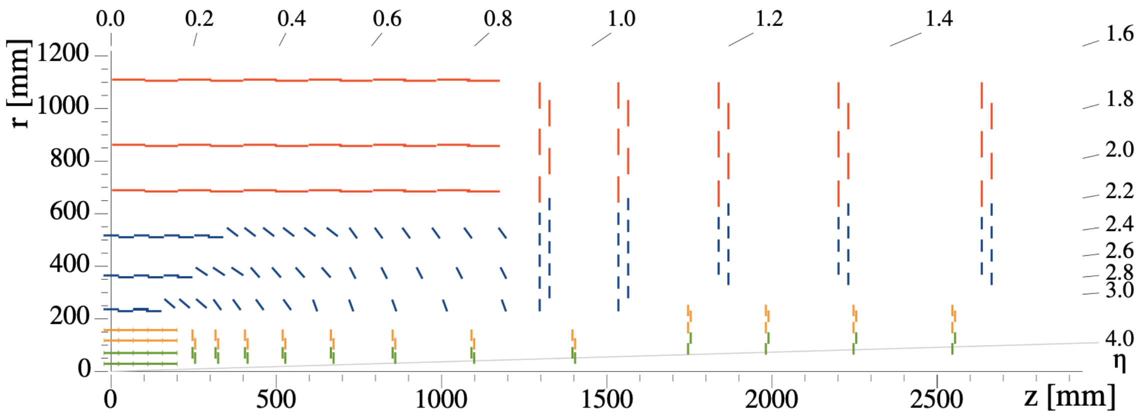
@HLLHC: Redoing frontend electronics for faster response

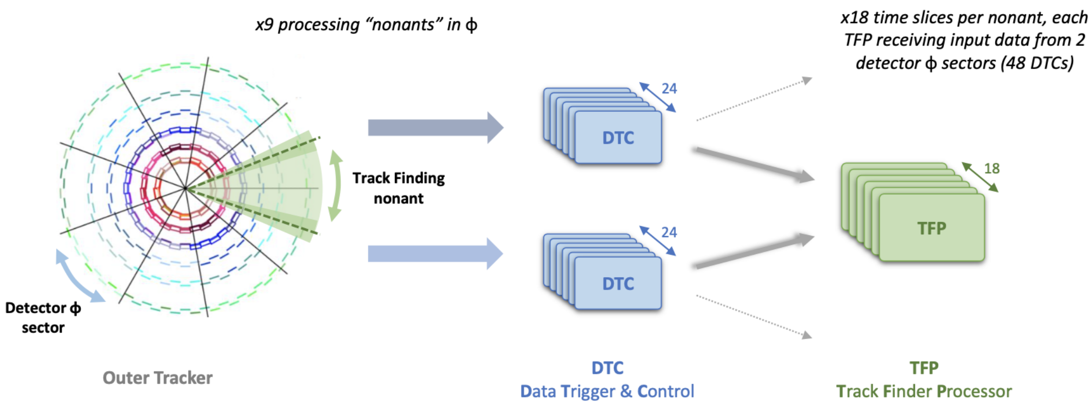
Getting the crystal data out (New for HLLHC)



There are 61200 crystals to be processed – packing 25 crystals per link out of BCP you still have 2448 links at 16 Gbps to contend in the calorimeter trigger path!

Getting the tracks out
(New for HLLHC)





Outer tracker double layers allow track stub readout

Tracklets formed in TFP consistent with >2GeV P_T propagated in-out, matched to form track candidates

Tracklets are then fit to make a track

Bits and Pieces from Everywhere

Detector	Object	N bits/object	N objects	N bits/BX	Required BW (Gb/s)
TRK	Track	96	1665	159 840	6 394
EB	Crystal	16	61 200	979 200	39 168
EB	Clusters	40	50	2 000	80
HB	Tower	16	2 304	36 864	1 475
HF	Tower	10	1 440	13 824	553
HGCAL	Cluster	250	416	104 000	4 160
HGCAL	Tower	16	2 600	41 600	1 664
MB DT+RPC (SP)	Stub	64	1 720	110 080	4 400
ME CSC	Stub	32	1 080	34 560	1 382
ME RPC	Cluster	16	2 304	36 864	1 475
ME iRPC	Cluster	24	288	6 912	276
ME GEM	Cluster	14	2 304	32 256	1 290
ME0 GEM	Stub	24	288	6 912	276
Total	-	-	-	-	62 593

Many Multi-gigabit Optical Links

Detector	TMUX period	Output links	Link speed (Gb/s)	Latency (μs)
Track Finder	18	$9 \times 2 \times 18 = 324$	25	5
ECAL	1	3060	16	1.5
HCAL	1	144	6.4	1.5
HF	1	36	6.4	1.5
HGCAL	18	$2 \times 3 \times 4 \times 18 = 432$	16	5
DT+RPC to BMTF	18	$60 \times 18 = 1080$	25	
DT+RPC to OMTF	1	72 (+18)	25	
RPC(endcap) to OMTF	1	42 (+6)	25	
RPC(endcap) to EMTF	1	48 (+12)	25	
CSC to OMTF	1	360 (+30)	3.2	1.75
CSC to EMTF	1	480 (+108)	3.2	1.75
iRPC	1	24 (+12)	16	
GEM (GE1/1)	1	96 (+12)	9.6	1.0
GEM (GE2/1)	1	36 (+12)	25	1.0
ME0	1	24 (+12)	25	

Xilinx – Ultrascale+ Processors

Product Tables and Product Selection Guides

Cost-Optimized Portfolio

Spartan-7	Spartan-6
Artix-7	Zynq-7000

7 Series

Spartan-7	Artix-7
Kintex-7	Virtex-7

UltraScale

Kintex UltraScale	Virtex UltraScale

UltraScale+

Kintex UltraScale+	Virtex UltraScale+

	Kintex UltraScale+	Virtex UltraScale+
Max System Logic Cells (K)	1,143	3,780
Max Memory (Mb)	70.5	65,913
Max DSP Slices	3,528	12,288
Max Transceiver Speed (Gb/s)	32.75	32.75
Max I/O Pins	572	832

Multi-gigabit-per-second serial links

WISCONSIN
UNIVERSITY OF WISCONSIN–MADISON

	Type	Max Performance[1]	Max Transceivers	Peak Bandwidth
Virtex UltraScale+	GTY	32.75	128	8,384 Gb/s
Kintex UltraScale+	GTH/GTY	16.3/32.75	44/32	3,268 Gb/s
Virtex UltraScale	GTH/GTY	16.3/30.5	60/60	5,616 Gb/s
Kintex UltraScale	GTH	16.3	64	2,086 Gb/s
Virtex-7	GTX/GTH/GTZ	12.5/13.1/28.05	56/96/16[3]	2,784 Gb/s
Kintex-7	GTX	12.5	32	800 Gb/s
Artix-7	GTP	6.6	16	211 Gb/s
Zynq UltraScale+	GTR/GTH/GTY	6.0/16.3/32.75	4/44/28	3,268 Gb/s
Zynq-7000	GTX	12.5	16	400 Gb/s
Spartan-6	GTP	3.2	8	51 Gb/s

HL-LHC → 25 Gbps

LHC → 10 Gbps

Key element - Multi-gigabit Opto-electronics

REVISION D

DO NOT SCALE FROM THIS PRINT

ESD SENSITIVE

TABLE 1: ASSEMBLY LENGTH LIMITS			
FIBER TYPE	HEAT SINK	MIN LENGTH (cm)	MAX LENGTH (cm)
-4	ANY	16	999
-5	-1,-2,-4,-5	12	100
	-3	12	48
-6	-1,-2,-4,-5	9	100
	-3	9	48

TABLE 2: LENGTH TOLERANCE	
ASSEMBLY LENGTH (cm)	TOLERANCE (cm)*
009-016	±0.16
017-999	±1%

* ROUNDED UP TO 2 DECIMAL PLACES

ECUO-B04-XX-XXX-0-X-1-X-XX

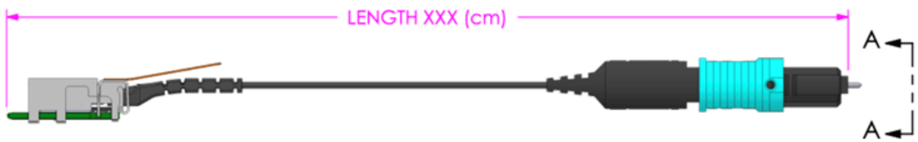
DATA RATE
-14: 14 Gbps
-25: 25.7 Gbps
-28: 28.1 Gbps

ASSEMBLY LENGTH
-XXX: LENGTH (cm) SEE TABLES 1, 2

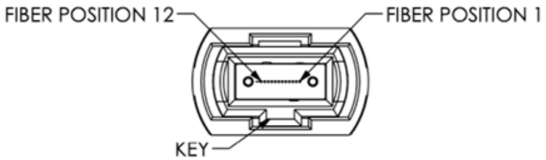
HEAT SINK
-1: FLAT
-2: PIN FIN
-3: FLAT WITH GROOVE (SEE NOTE 2)
-4: PCIe® PIN FIN (-14 DATA RATE ONLY)
-5: 1.75 cm TALL PIN FIN (-25 & -28 DATA RATES ONLY)

END OPTION
-01: MTP® MALE
-02: MTP® FEMALE
-07: MXC® INTERNAL PLUG
-0E: MPO PLUS® BAYONET MALE

FIBER TYPE
-4: AQUA LOOSE TUBE WITH BOOT
-5: BLACK JACKETED RIBBON WITH BOOT
-6: BLACK JACKETED RIBBON



PART NUMBER ECUO-B04-XX-XXX-0-1-5-01 SHOWN



VIEW A-A
END OPTIONS -01/-02/-0E

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETERS.
ALL DIMENSIONS ARE FOR REFERENCE ONLY

samtec
520 PARK EAST BLVD, NEW ALBANY, IN 47150
PHONE: 812-944-6733 FAX: 812-948-5047
e-Mail info@SAMTEC.com code 55322

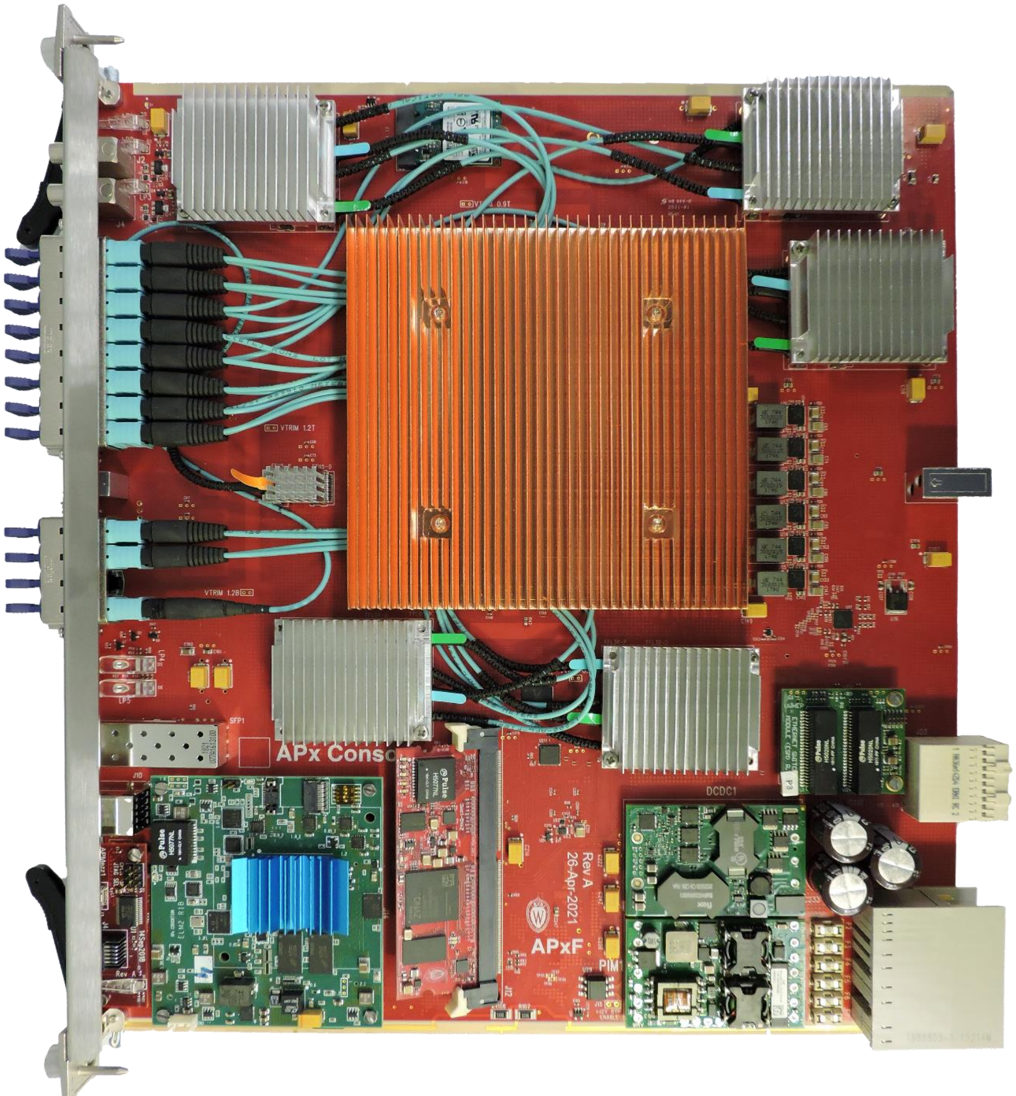
MATERIAL: DO NOT SCALE DRAWING SHEET SCALE: 1:1

DESCRIPTION: OPTICAL FIREFLY ASSEMBLY

DWG. NO. ECUO-B04-XX-XXX-0-X-1-X-XX

BY: JEAN W. 01/06/2016 SHEET 1 OF 6

Advanced Processor Prototype for HL-LHC



TIFR built IPMC &
ESM mezzanines

Wisconsin APxF Board

Xilinx VU13P or VU9P FPGA

ZYNQ-IPMC
(ATCA IPMI controller)

ELM (ZYNQ-based
embedded Linux endpoint)

ESM (GbE switch)

High efficiency heatsinks

Front-panel inputs

25G Samtec Firefly positions
loaded – 10x12 + 1x4
(124 25 Gbps links)

APx – Firmware/Software

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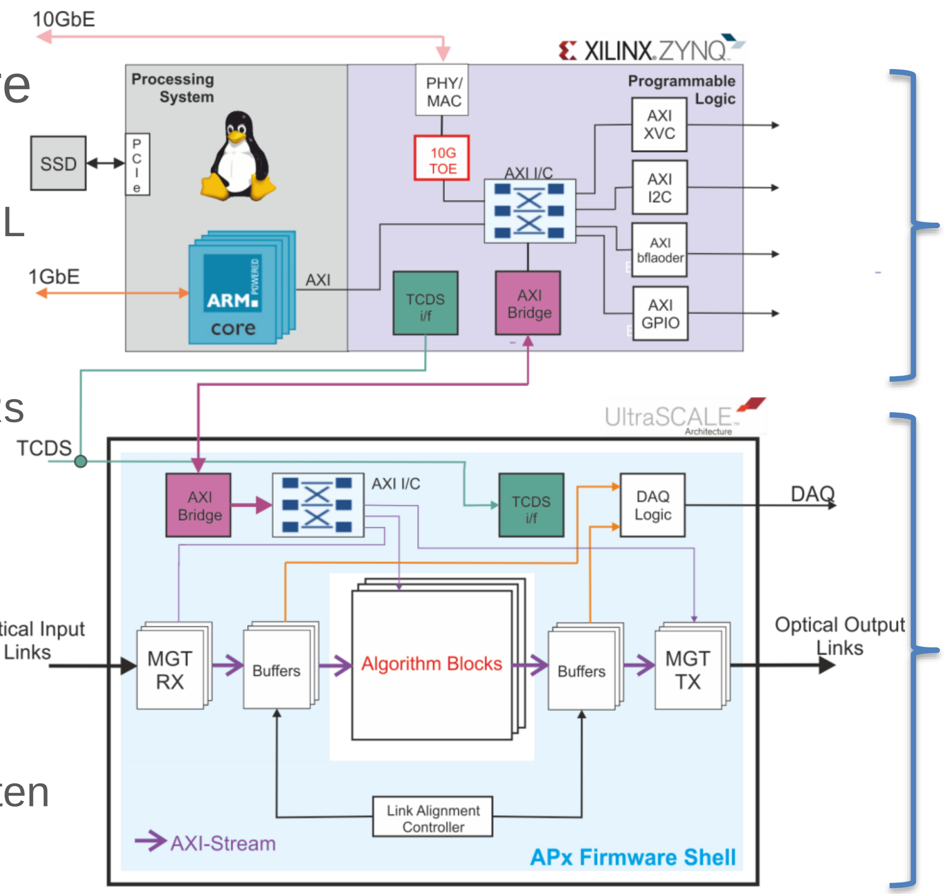
A new paradigm for firmware development

- Core firmware written in VHDL by engineers
- Gigabit link support
- Data exchange between SLRs within chip
- Test buffers
- Clock and control

Physics

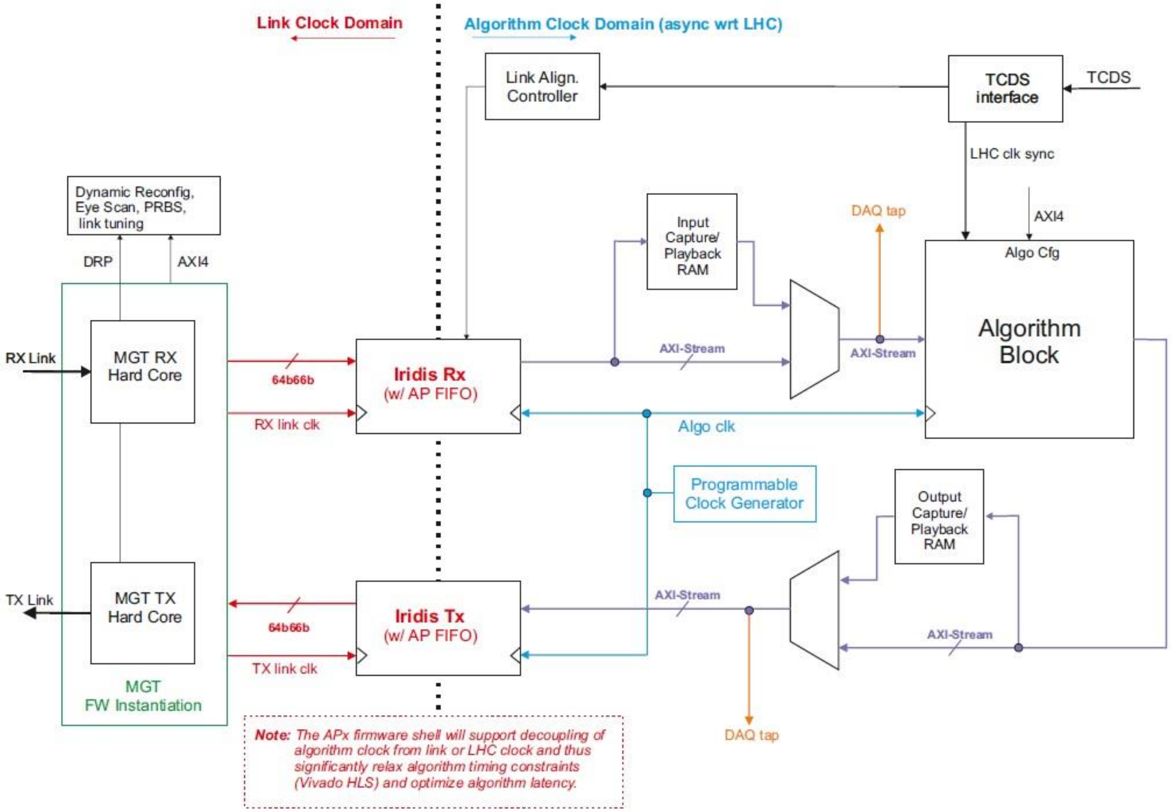
- Algorithmic firmware in high-level languages like C++ written by physicists



ELM:
Control endpoint, providing complete board overhead functionality

Processing FPGA:
- I/O
- data processor
- DAQ

APx Firmware Shell



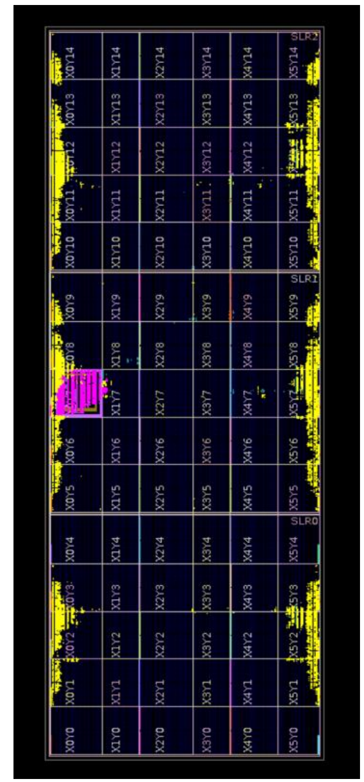
APx-FS Resource Utilization

Utilization VU9P build Post-Synthesis | **Post-Implementation**

Graph | **Table**

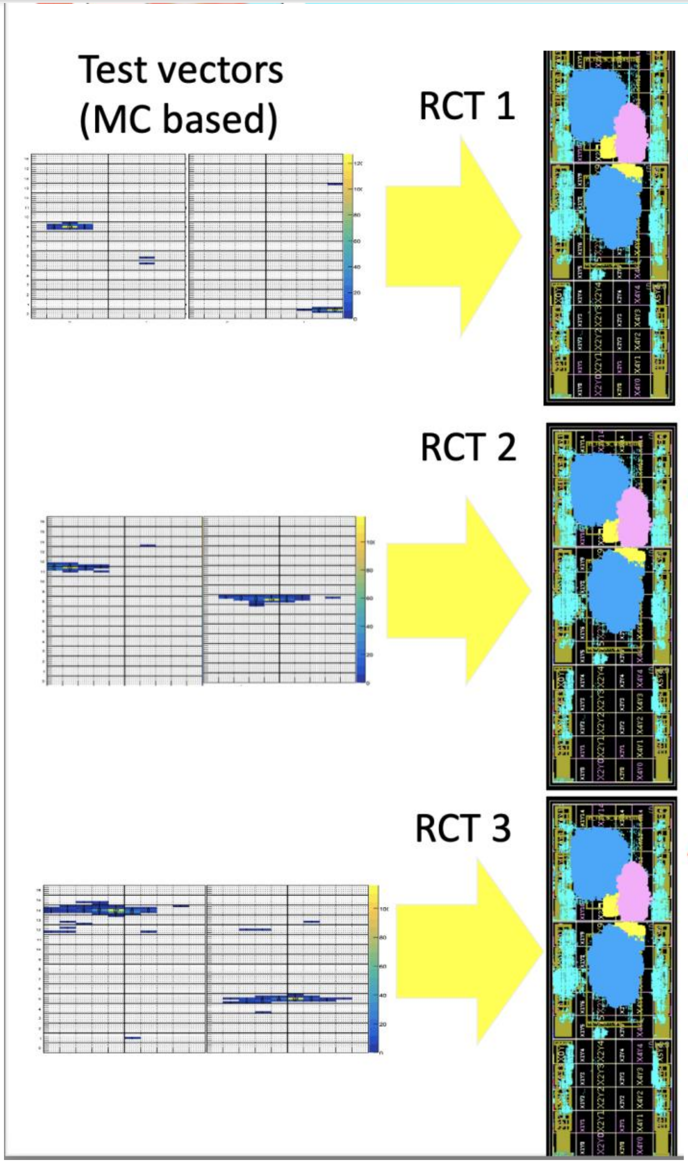
Resource	Utilization	Available	Utilization %
LUT	33309	1182240	2.82
LUTRAM	963	591840	0.16
FF	51563	2364480	2.18
BRAM	7	2160	0.32
IO	9	416	2.16
GT	102	104	98.08
BUFG	236	1800	13.11
MMCM	3	30	10.00

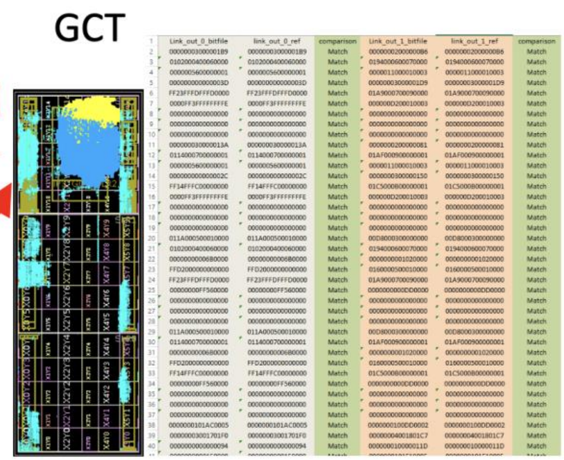
- 100x 25G GTY links w/ support infra
- Central AXI infra with MGT-based Chip2chip core



APd1 VU9P FPGA floorplan

Calorimeter Firmware Tests



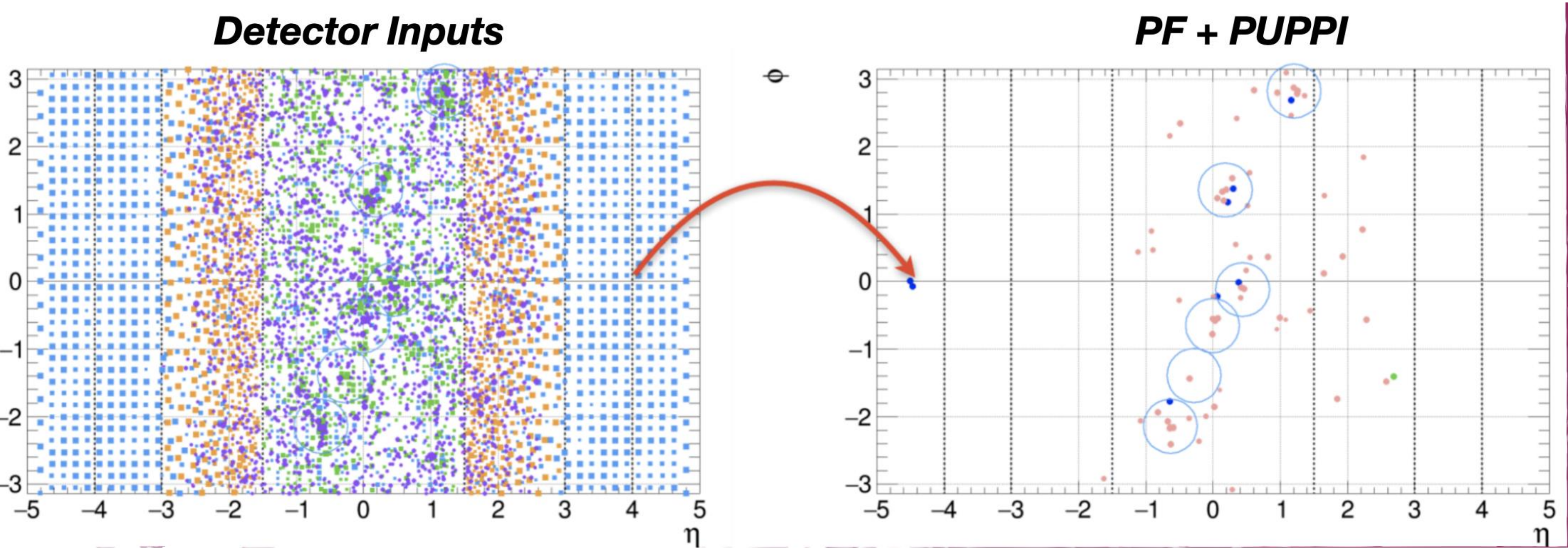


GCT HW output
compared to expected

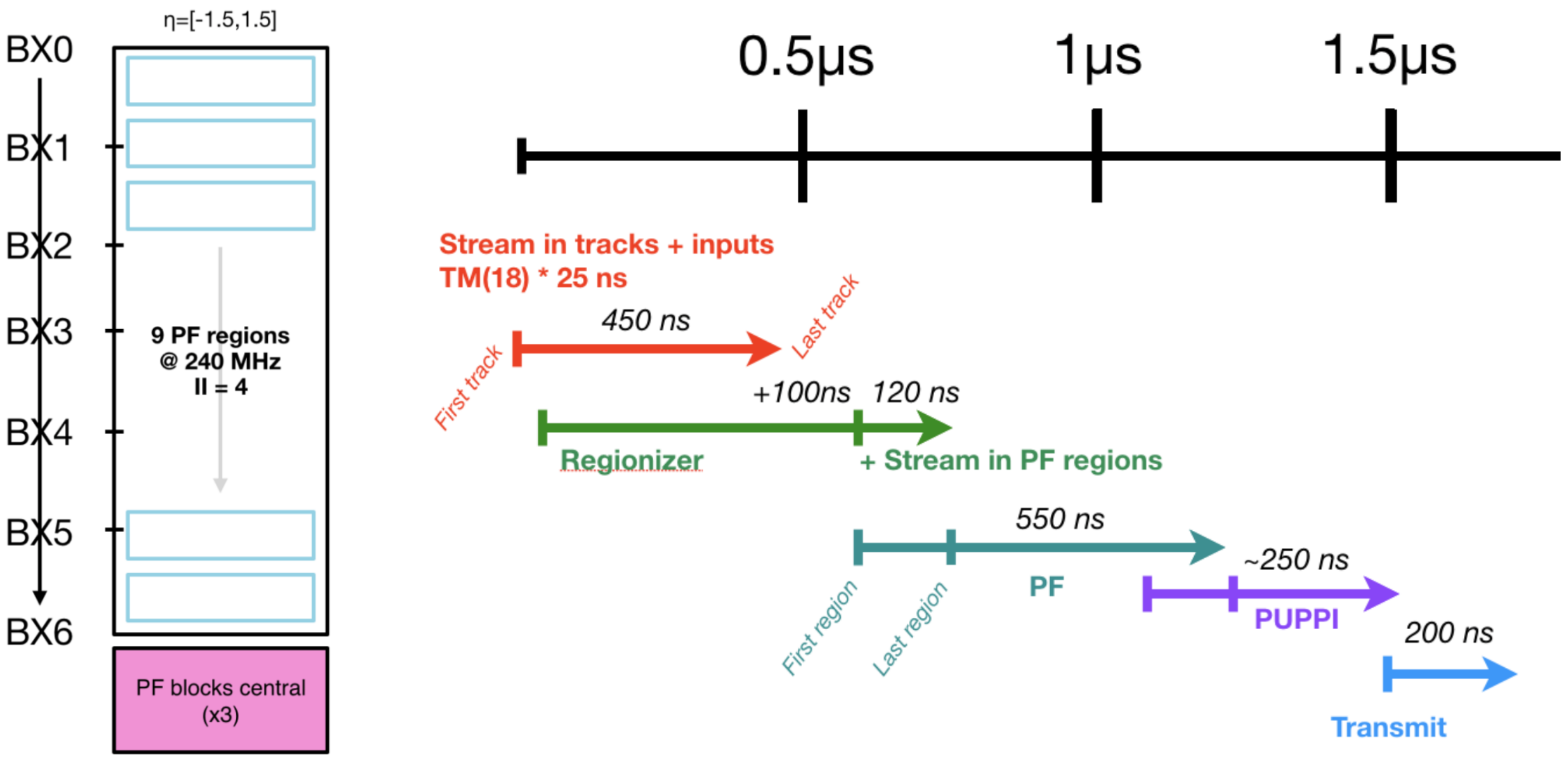
First time capturing real
data in multiple card test!

Firmware prepared and tests conducted by U of Hyderabad student Piyush Kumar

Particle Flow Reconstruction on FPGAs



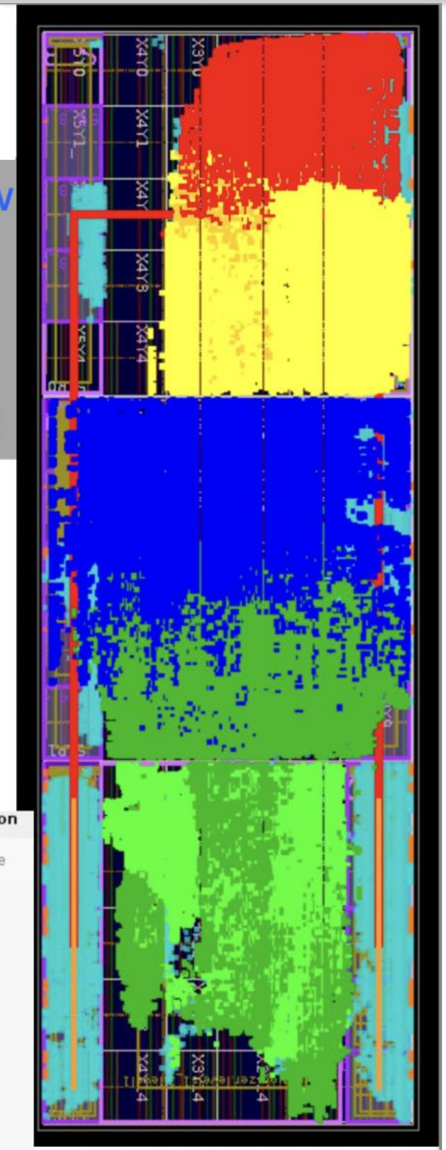
Particle Flow Implementation

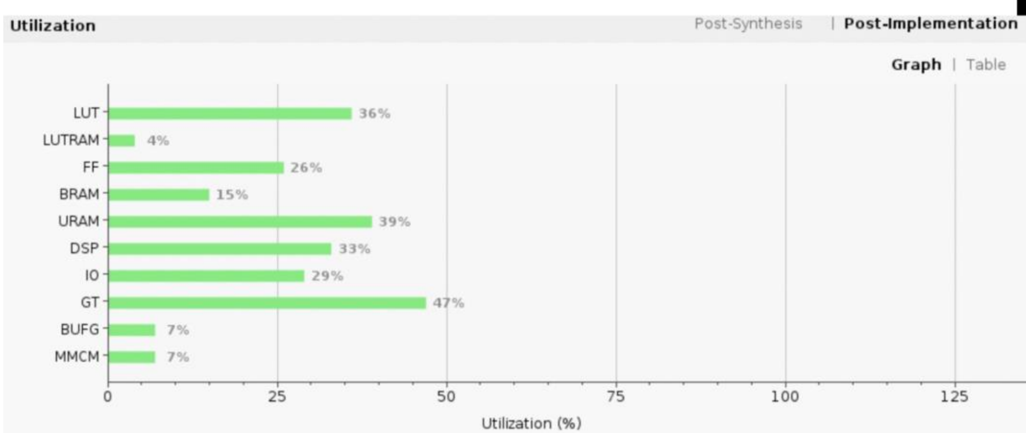


Particle Flow – Correlator Layer 1

- Five firmware pieces in main algorithm:
  - Common APx infrastructure
  - Regionizer
  - Particle Flow (PF)
  - PileUp Per Particle Identification (PUPPI)
  - Output sorting
- Meets timing with <50% resource use for VU9P-2 (plan to use VU13P-2).
- Latency of 1.1 μs is sufficient to meet the requirements
- Simulation and emulation match in single board tests.
- The most challenging firmware project we have, and it works!
- Additional algorithm to do e/γ preprocessing tested; not yet integrated

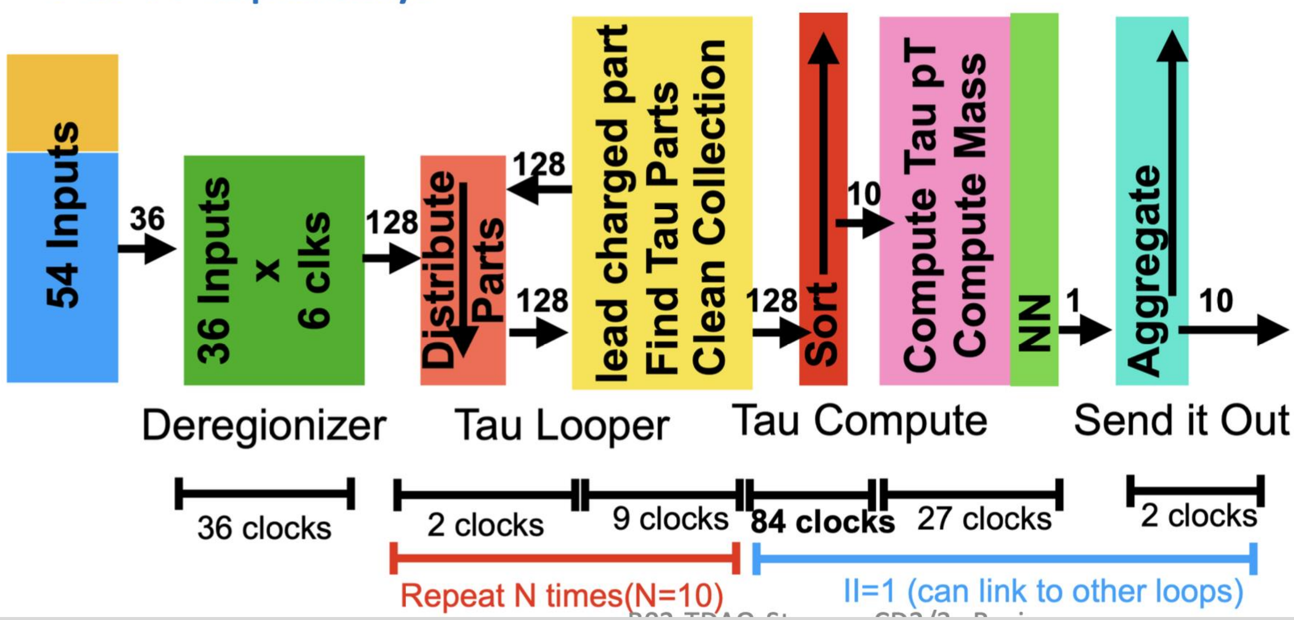
particle flow
PUPPI
output sort
regionizer 1
regionizer 2

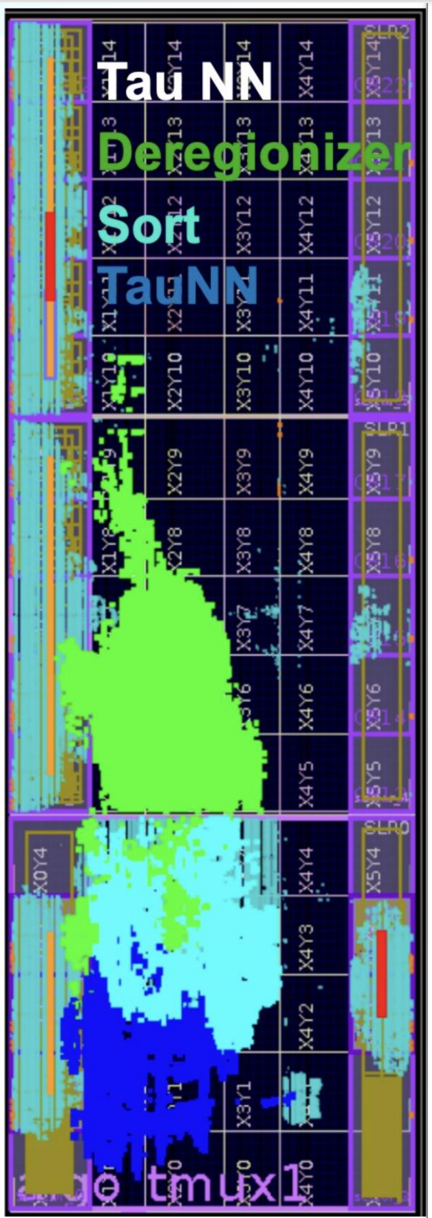




Particle Flow – Correlator Layer 2 τ_h

- τ reconstruction with neural net:
  - One of the first CL2 algorithms
  - Now uses redesigned firmware incorporating deregionizer code and seeded cone jet reconstruction before τ_h identification.
  - Meets timing
  - Latency of 1.0 μs is sufficient to meet requirements
  - Emulation matches and is in CMSSW with multi-vertex PUPPI capability.





Anatomy of Example Algorithm

Bitonic sort

- **Parallel** algorithm for sorting
- compare elements in a **predefined sequence** and the sequence of **comparison doesn't depend on data**
- suitable for implementation in hardware
- N-input bitonic sorting unit has $\log_2(N) \times (\log_2(N) + 1)/2$ CAE stages
- the total number of CAE blocks in an N-input bitonic sorting unit is $N \times \log_2(N) \times (\log_2(N) + 1)/4$
- For **32 input** bitonic sorting unit require **15 CAE stages** and **240 CAE block**.

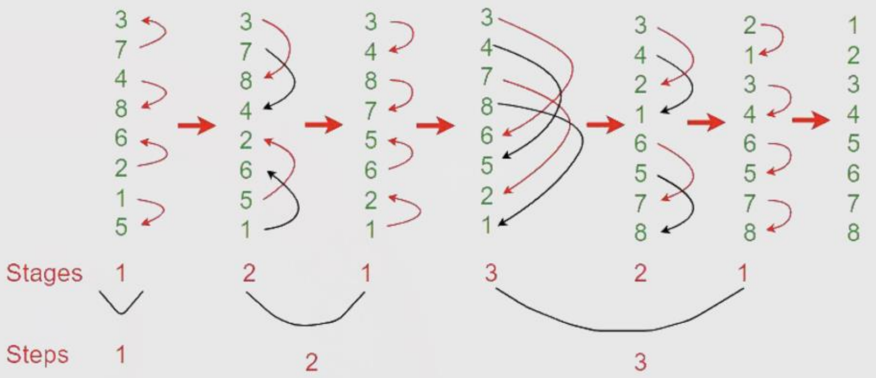


Fig 1: Bitonic sorting

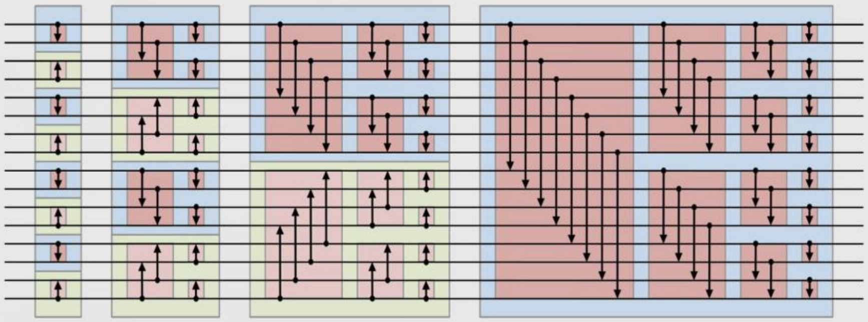
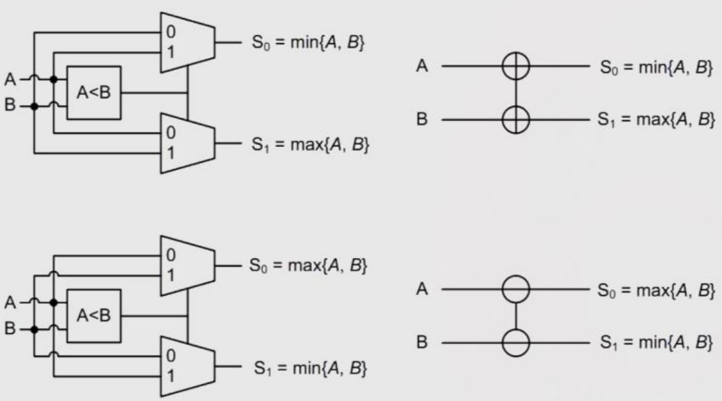


Fig 2: Bitonic sorting and sorting network of 16 IO

Use of C++ & High Level Synthesis

Compare & Exchange block (CAE)

https://github.com/piyushkumarhcu/Bitonic-Sort-32IO




```
//Main CAE block (compare and exchange)
GreaterSmaller AscendDescend(const din_t &x, const din_t &y){
#pragma HLS PIPELINE II=9
#pragma HLS INLINE
    GreaterSmaller s;

    s.greater = (x > y) ? x : y;
    s.smaller = (x > y) ? y : x;

    return s;
}
```

Timing & Latency

HLS Implementation

- This algorithm is implemented in Vivado-HLS for 32 IO
- Synthesized for Virtex UltraScale+ FPGA (xcvu9p-flgc2104-1-e)
- Target clock frequency is 360 MHz
- Latency of 9 clock cycle
- *https://github.com/piyushkumarhcu/Bitonic-Sort-32IO*

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	2.78	1.890	0.83

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
9	9	9	9	function

Fig 4: Timing information

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	20164	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	65	-
Register	-	-	9307	-	-
Total	0	0	9307	20229	0
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	0	0	~0	1	0
Utilization SLR (%)	0	0	1	5	0

Cosimulation Report for 'bitonicSort'

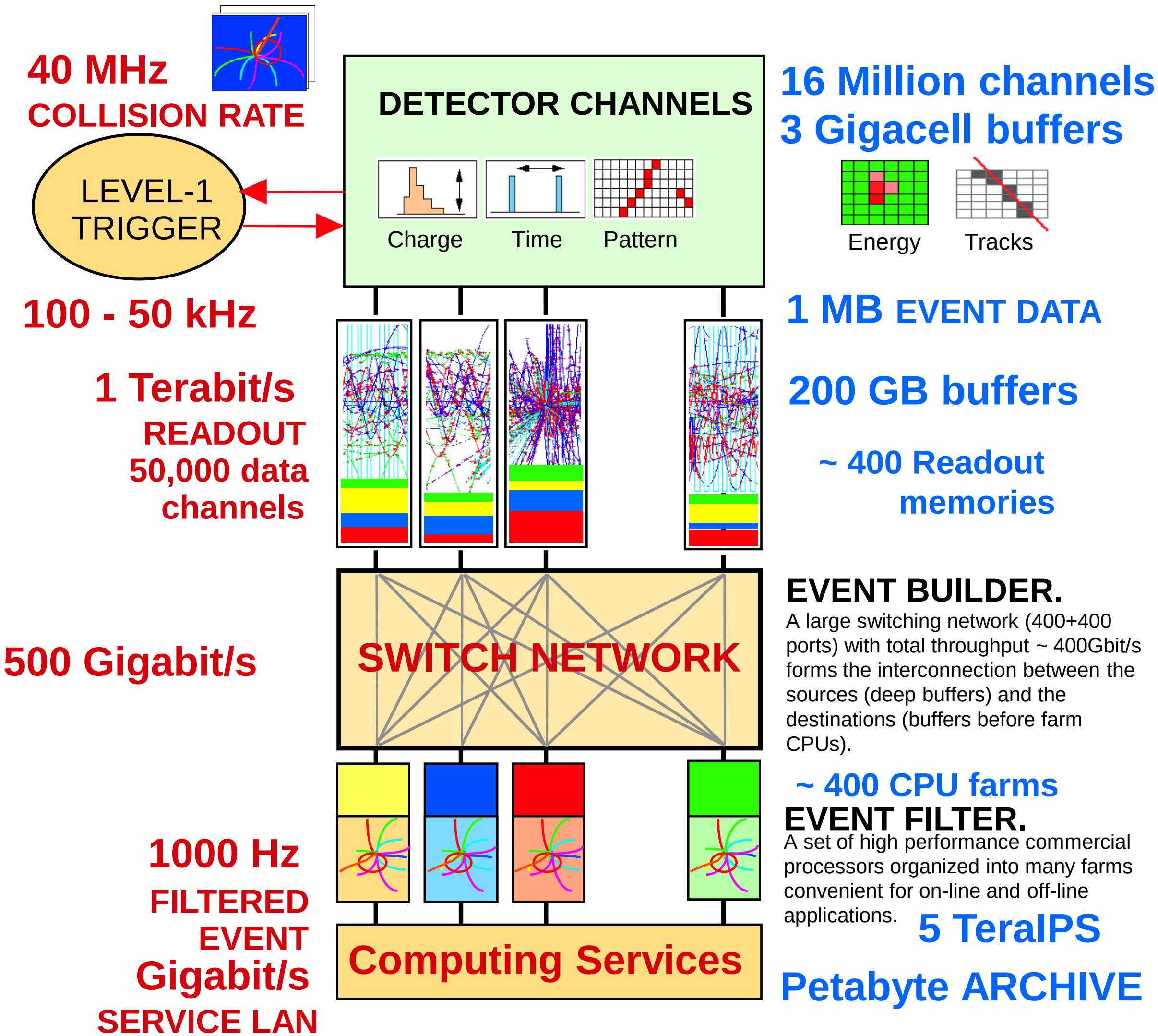
Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	9	9	9	NA	NA	NA

Fig 4: Utilization summary and cosimulation result

Event Builder & High-Level Trigger

Current System



Challenges:

1 GHz of Input Interactions

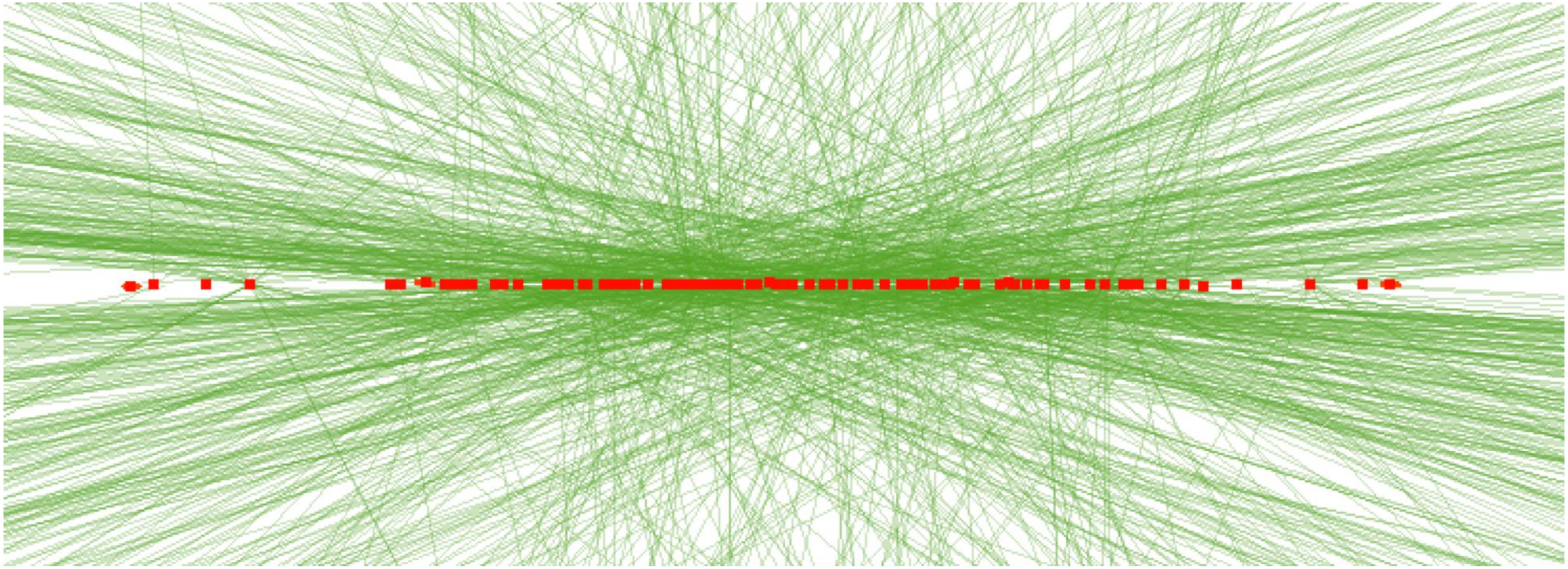
L1 Trigger selection 100 kHz

Build events

Process fully and select events

Archival Storage at about 1000 Hz of 1 MB events

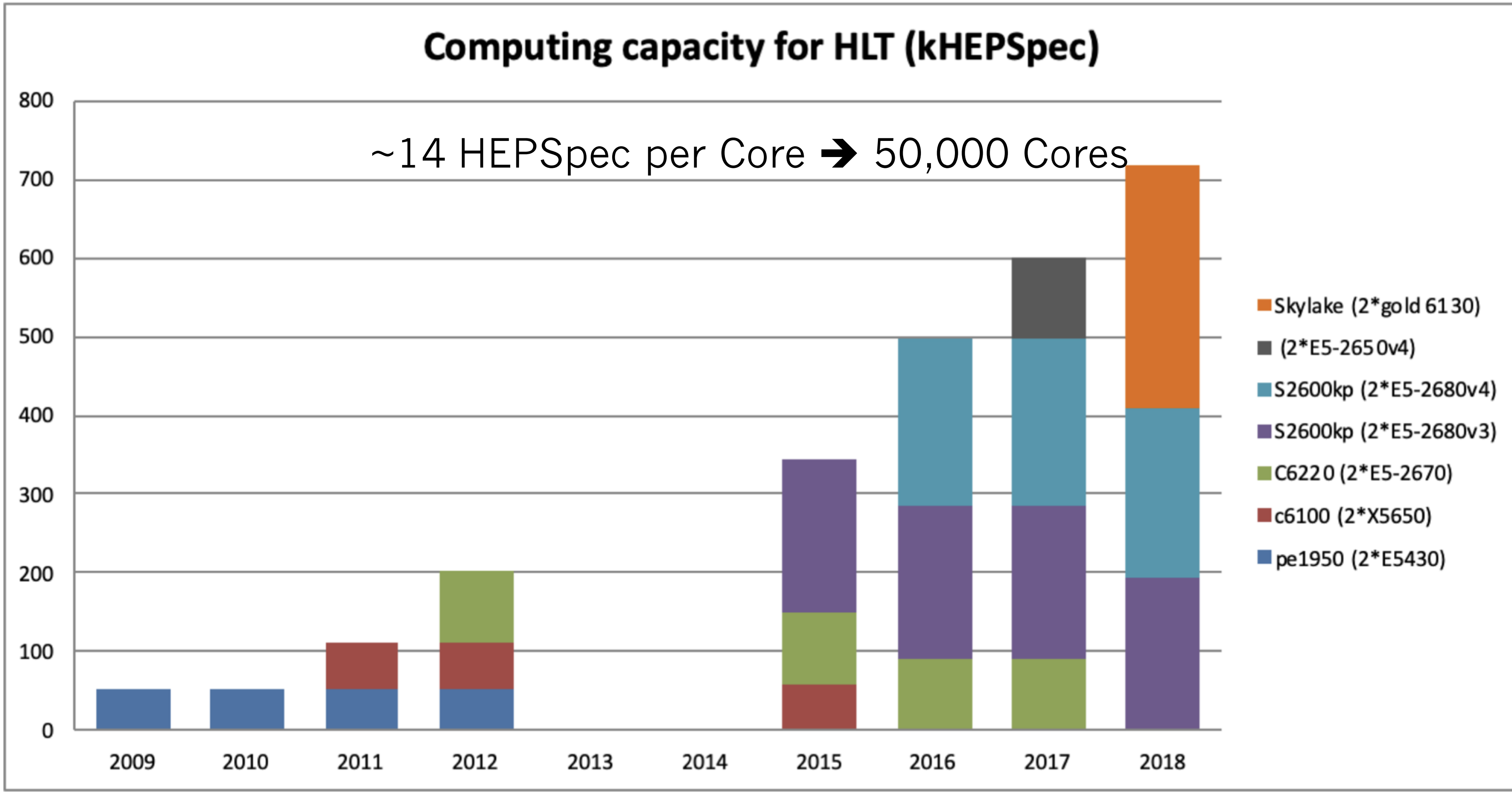
HL-LHC Computing Challenge



- HL-LHC with greater beam intensities results in per-event pileup of 140-200, compared to 30-40 today
- Maintaining the low trigger thresholds necessary for the physics program leads to an increase in trigger input rates from 100 kHz to 750 kHz ; output rates from 1 kHz today to 7.5 kHz from 2025
- Busier events are larger and take ~16 more time to reconstruct

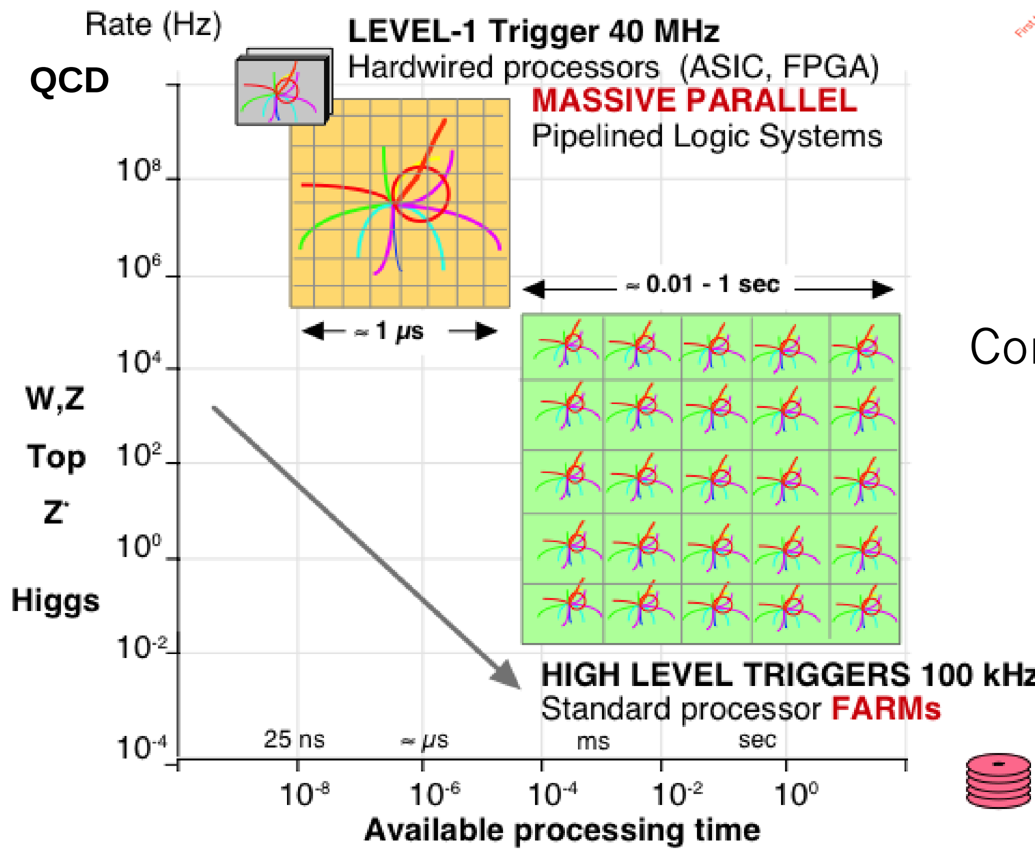
High Level Triggers – Online CPU

Process ~100 kHz input and select 1000 Hz output to storage systems

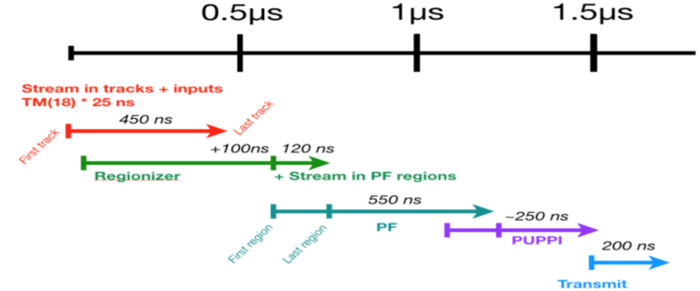


- Added capacity as pileup increased

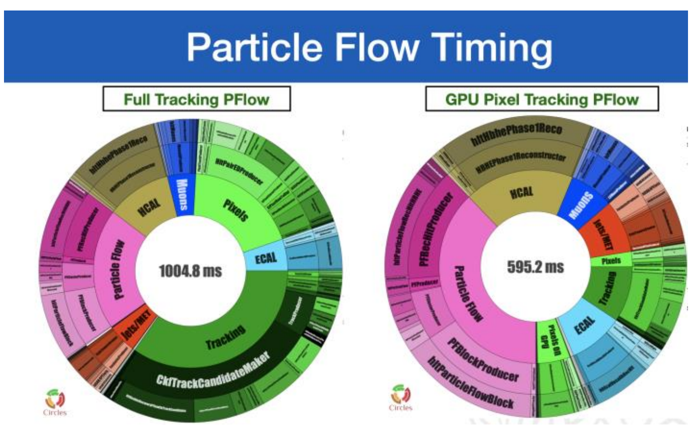
Processing HLLHC Data



Custom Processors (μs) – L1 Trigger

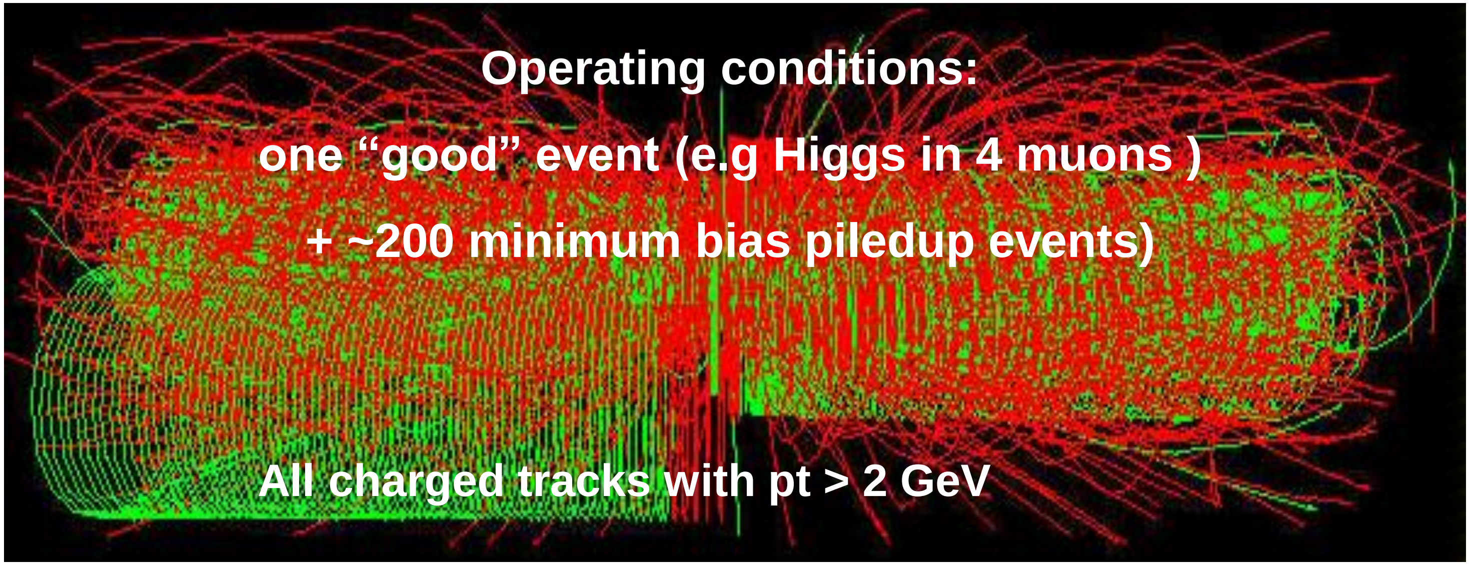


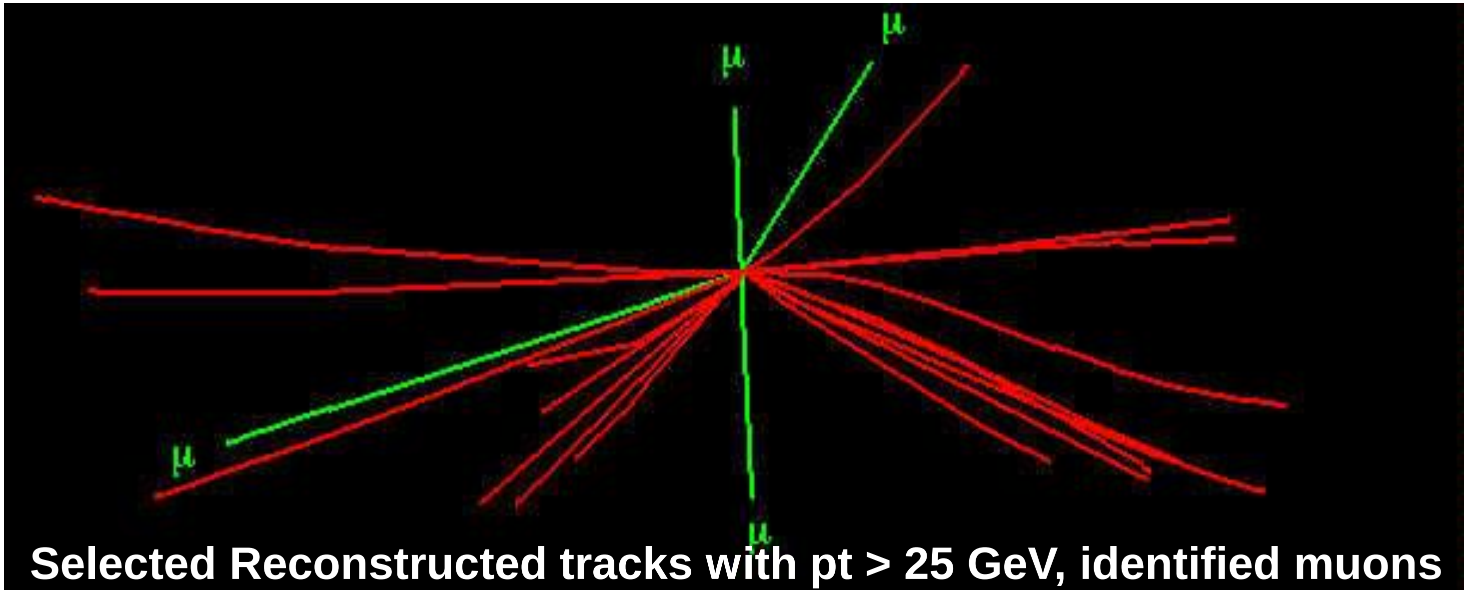
Commercial Processors (600ms – 1s) High Level Trigger



GPU Usage

Event Reconstruction & Tagging





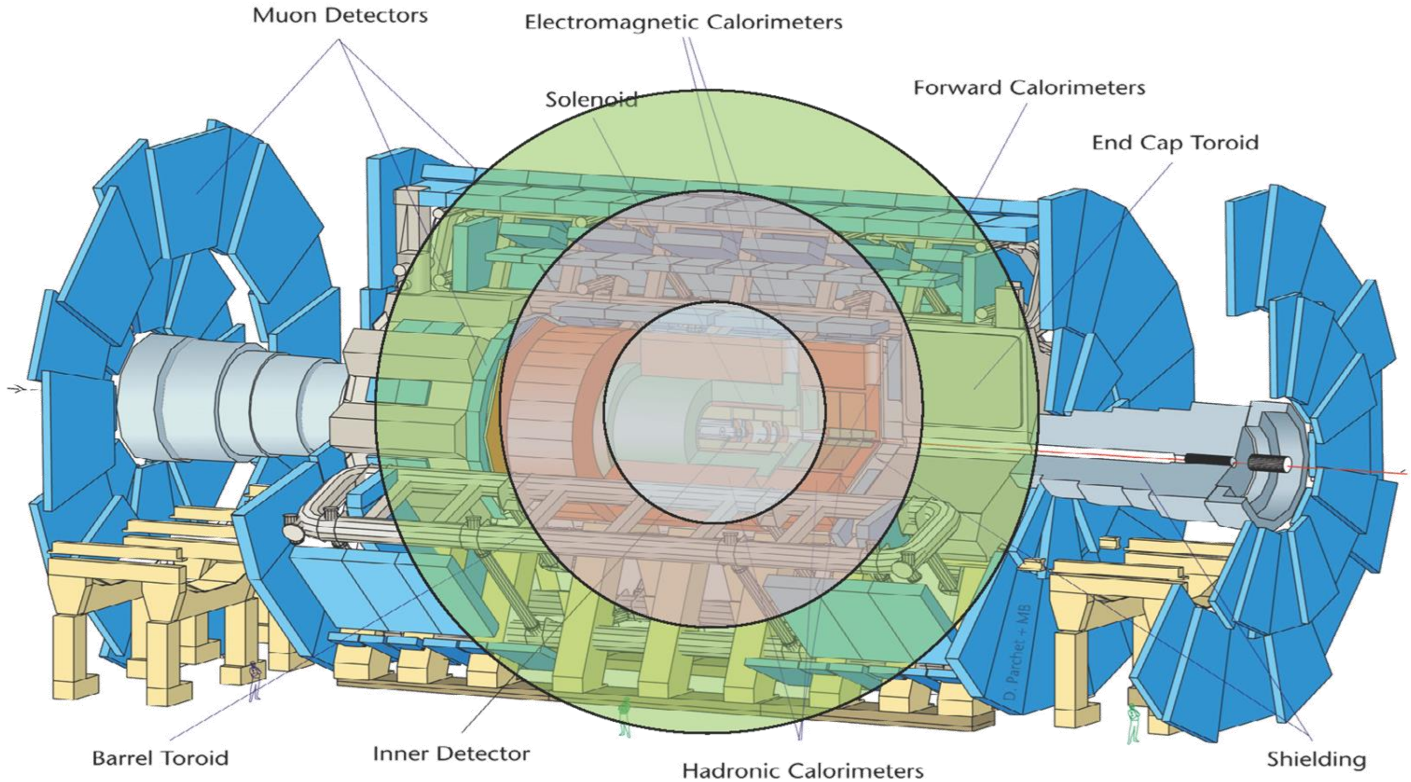
100s of milliseconds of processing on modern Commodity CPUs from Intel or AMD

New Timing Detectors

Divide and conquer
In space and time

Building in Timing Detectors to exploit timing information to mitigate pileup

c = 30 cm/ns → in 25 ns, s = 7.5 m



These timing Detectors are not in L1 trigger but in HLT
Mitigate pileup & Access to Long lived particles

Concluding Thoughts

We in HEP are not innovators of modern computing technologies but we are amongst those who push it the most.

A team of engineers and physicists have tamed the LHC data deluge with intelligent use of telecommunications and computing technologies to enable fundamental physics discoveries.

We continue to push the technologies to the limit.

Advances in telecommunications and computing technologies are continually adapted to track increasing data volumes.

Students and postdocs are getting good training, especially in operations and firmware, for potential careers in both academia and industry – We invite you to join us in the HL-LHC adventure!