The CALOROC ASICs for multi-channel SiPM readout

Workshop: Exploring the Positronium Frontier

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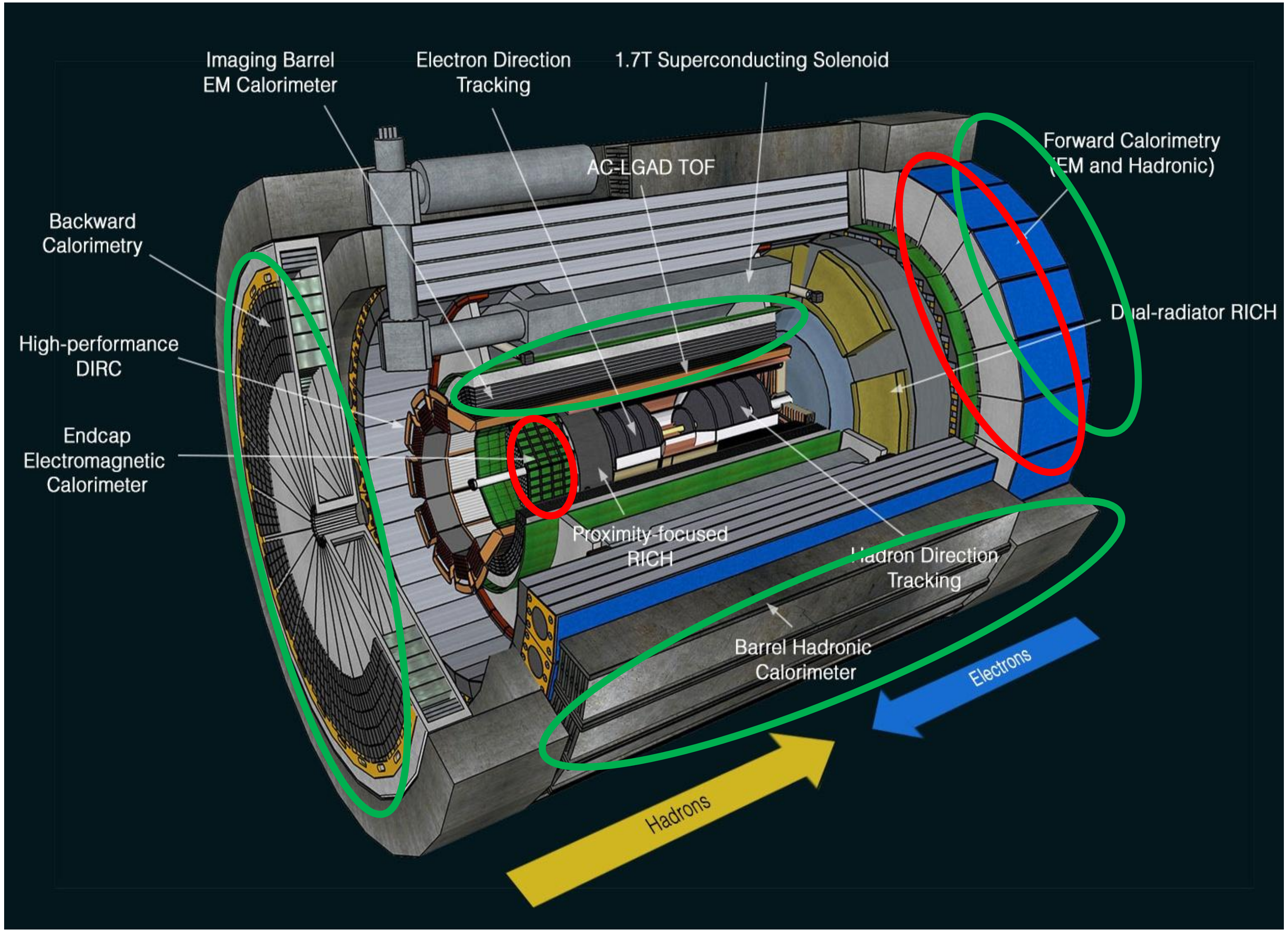
February 12, 2026

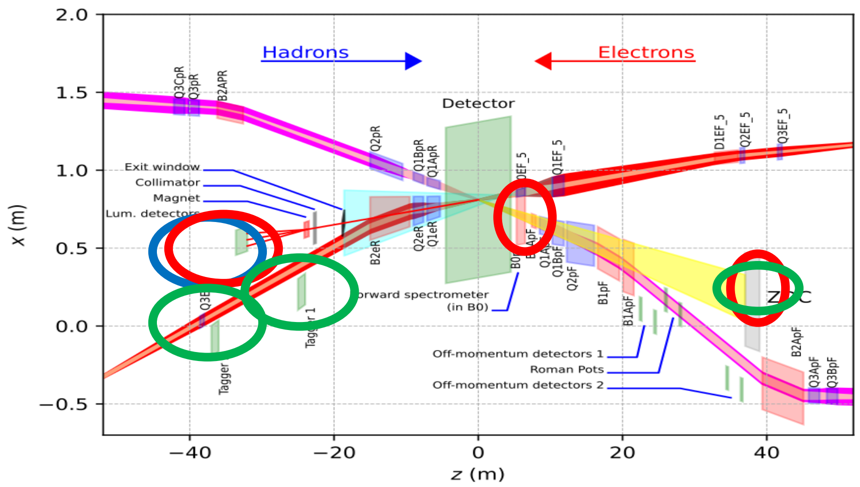
Calorimetry at ePIC



13 Calorimeters:

- 7 x SiPM – CALOROC
- 5 x SiPM – Discrete
- 1 x SiPM – Commercial fADC250

From J. Landgraf (IDR review)



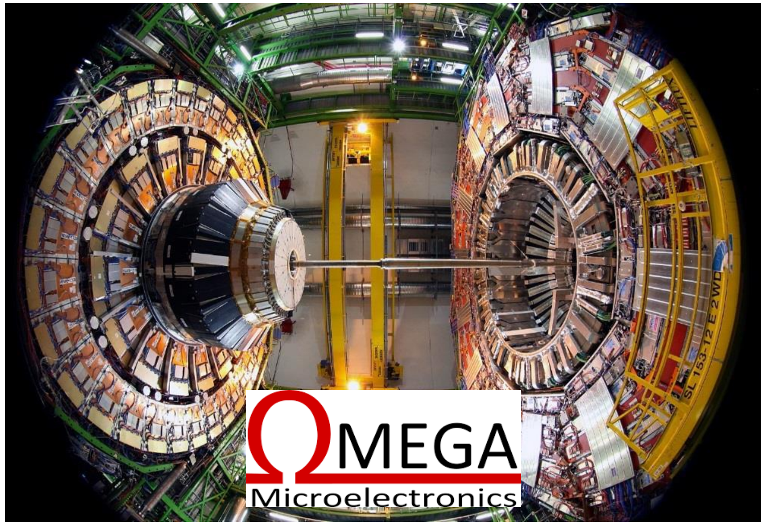
H2GCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year

CALOROC for EIC



Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

Common interfaces

HEP trend => imaging calorimetry

- High number of channels
- Charge and precise timing (<100 ps)
- Low power + System-On-Chip

Based on H2GCROC, CALOROC will provide a versatile and low-power solution for SiPM readout

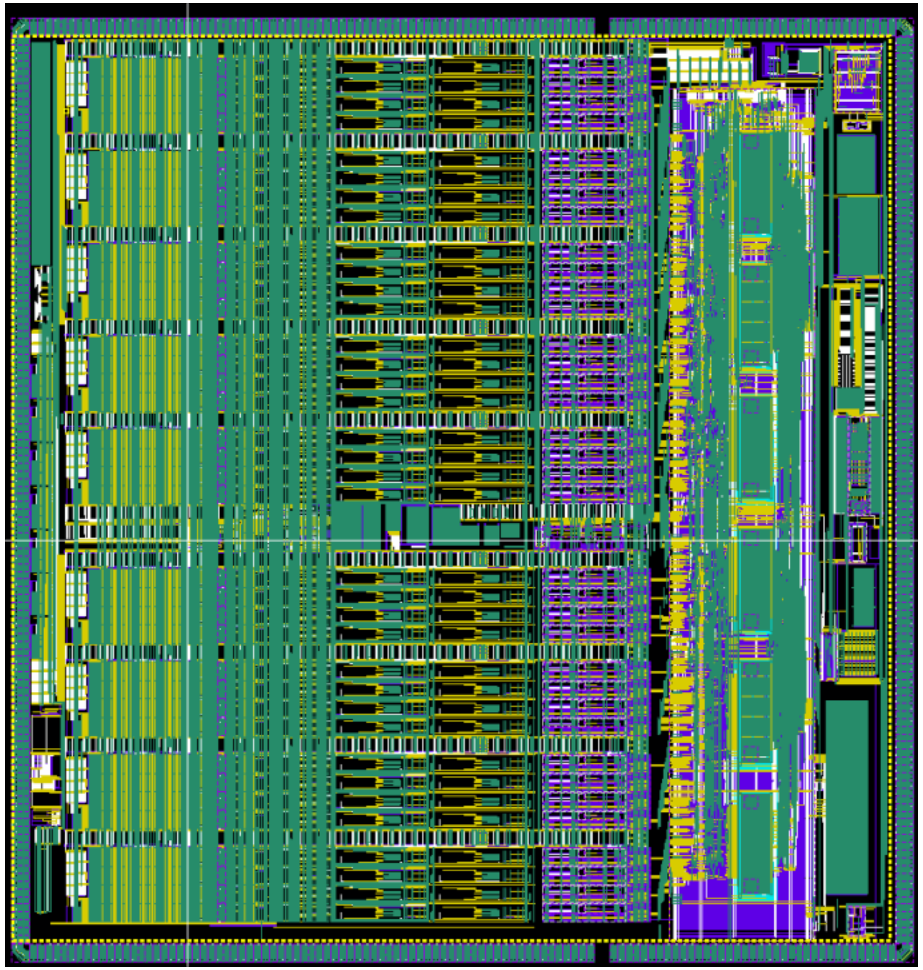
Overview of CALOROC family : 1A/1B/1C

- **CALOROCs common features**
  - 36 channels ~10-15 mW/ch, charge and time measurement
  - Auto-trigger and Streaming readout : 2 links @ 1.28 Gb/s
  - Triplicated I2c configuration and fast commands inputs
  - TSMC 130nm technology
  - BGA package : same pinout

- Conservative **CALOROC1A**: SiPM readout from H2GCROC
  - SiPM range capa from 230 to 560 pF

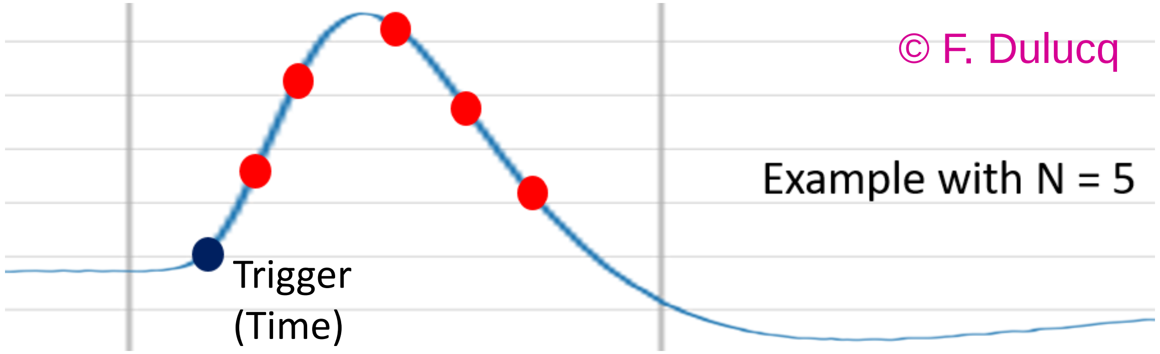
- New **CALOROC1B**: SiPM readout with gain switching
  - SiPM range capacitance from 560 pF to 10 nF
  - New analog front end : higher dynamic range and input capacitance
  - Lower noise, better jitter and timing performance

- **CALOROC1C** for Si/LAr detectors: Si readout from HGCROC
  - Slower shaping
  - Cryogenic temperature adjustment



CALOROC: Waveform Digitizer with Auto-Trigger

- CALOROC is a waveform digitizer working @ 40 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm is outside (back-end or offline)



CALOROC can accept ~ 50 (100) kHz rate per channel

Internal CALOROC memory writing is without dead time

Hit-rate is only limited by serial link bandwidth

A zero-suppress feature can be activated

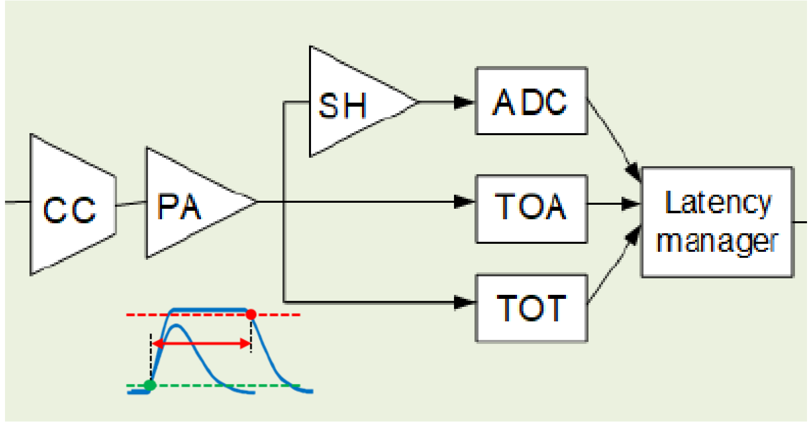
A fast command can trigger an ASIC snapshot

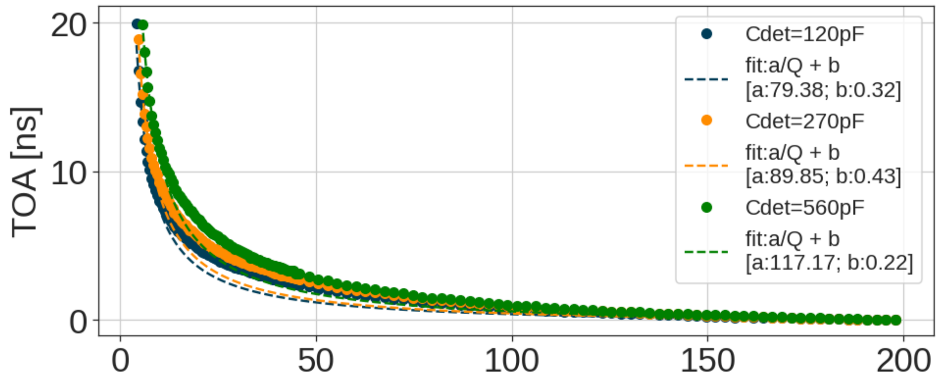
(monitoring, calibration, heartbeat)

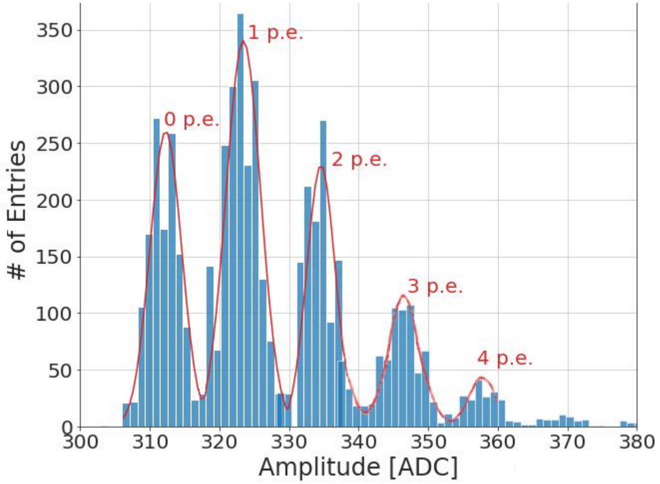
CALOROC1A (based on H2GCROC)

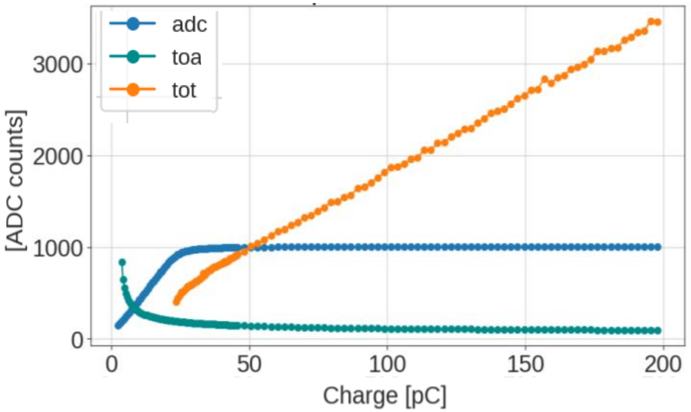
- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / Radiation performance / SiPM capacitance range 100-600 pF

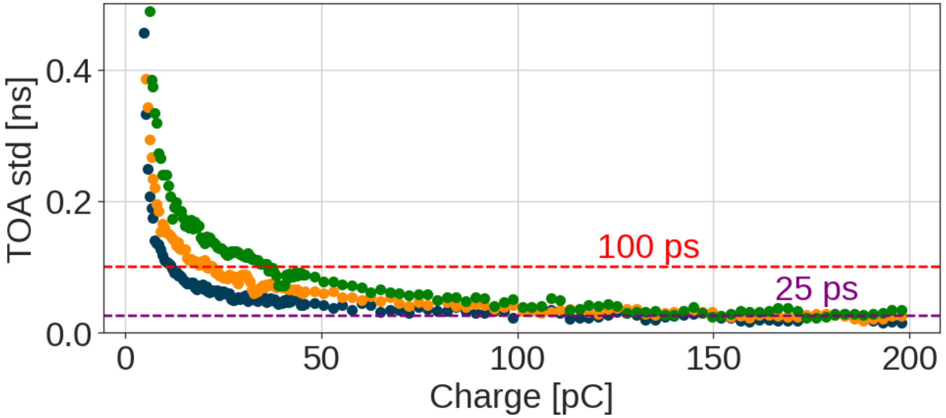
© J. Gonzalez

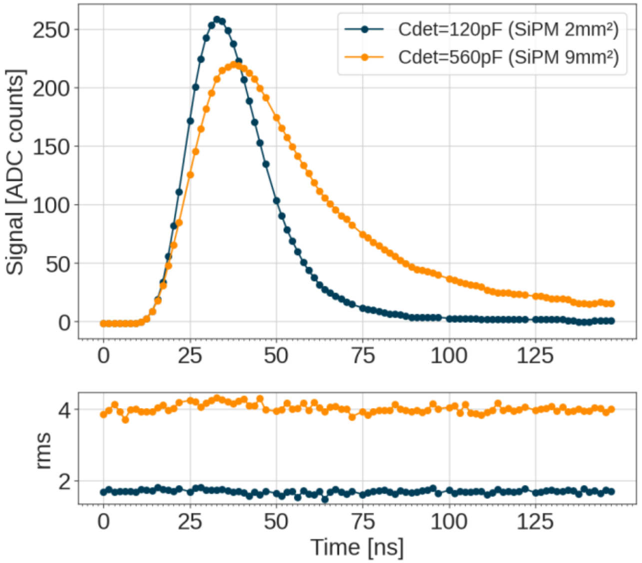










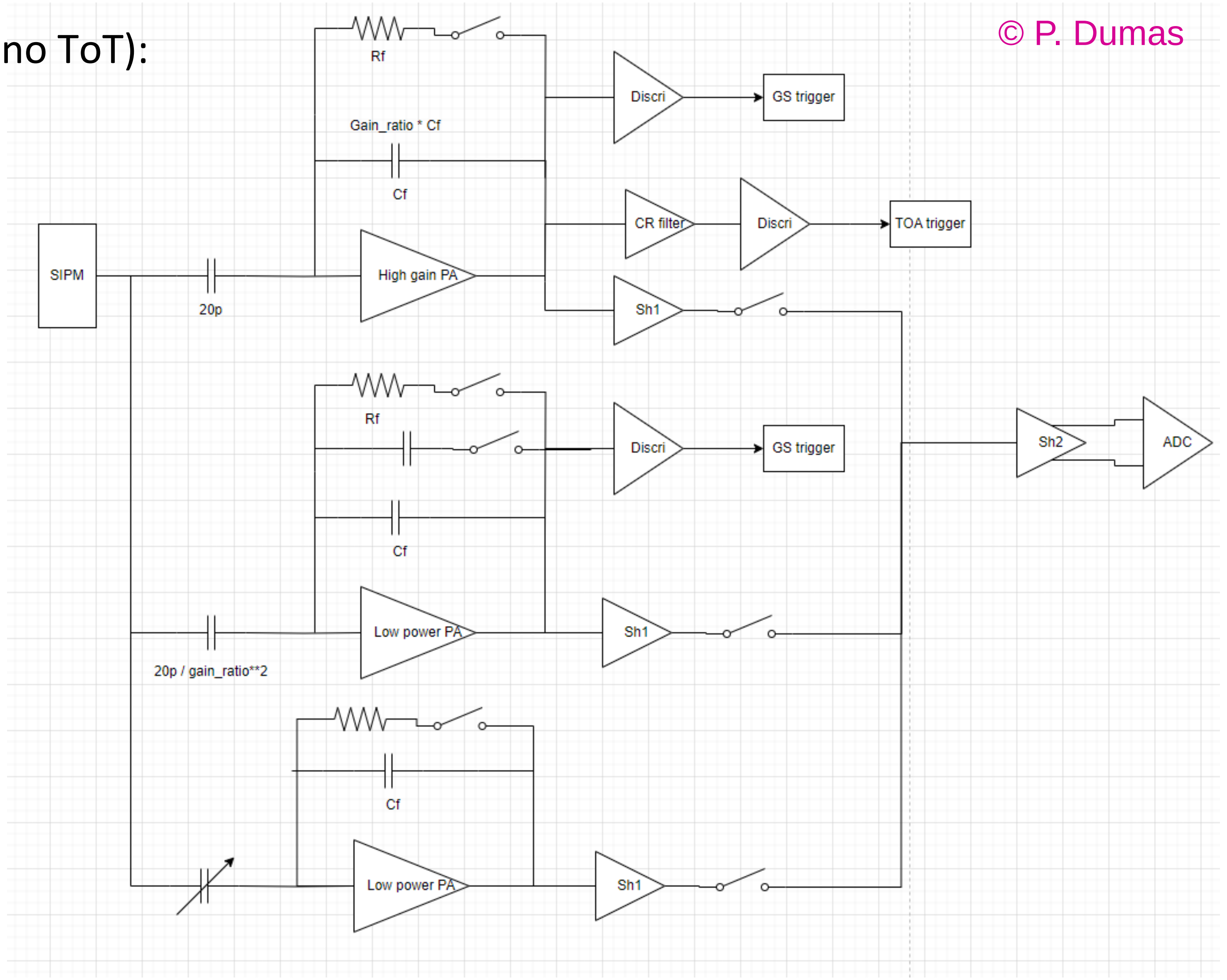


- CALOROC1A will only update its back-end to be EIC compatible

* TWEPP 2023 → https://doi.org/10.1088/1748-0221/19/04/C04005

CALOROC1B: gain switching architecture

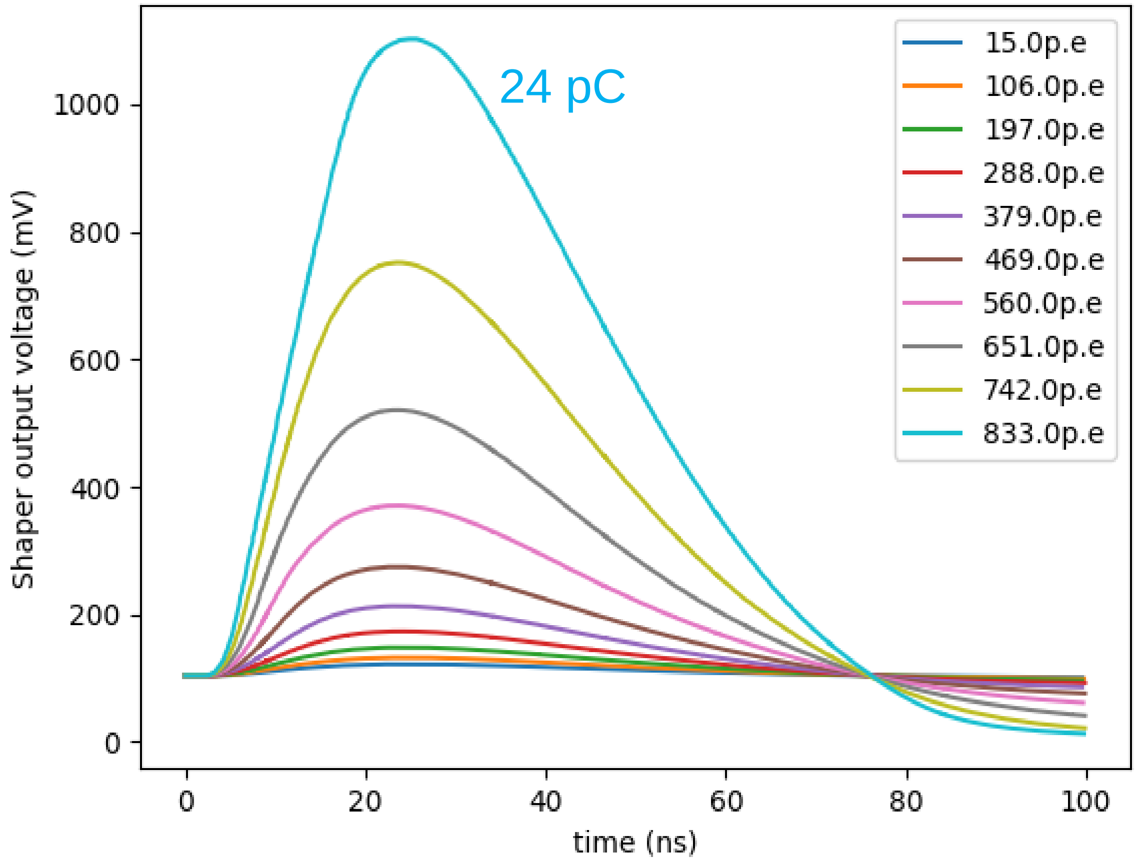
- New dynamic frontend with switched gain (no ToT):
  - High gain, 2x medium gains, Low Gain
  - Voltage gain architecture: high impedance input
    - Limitation: $V_{in\_max} = Q_{max}/C_{SiPM}$
- Reuse CMS-H2GCROC ADCs and TDCs:
  - 10-bit 40 MHz ADC (Krakow)
  - 25 ps TDC (Saclay)
- Shared CALOROCs backend
- Common specifications:
  - SiPM from 500 pF to 2.5 - 10 nF
  - ~ 10 mW/channel
  - CMS HL-LHC Radiation level 200 Mrad



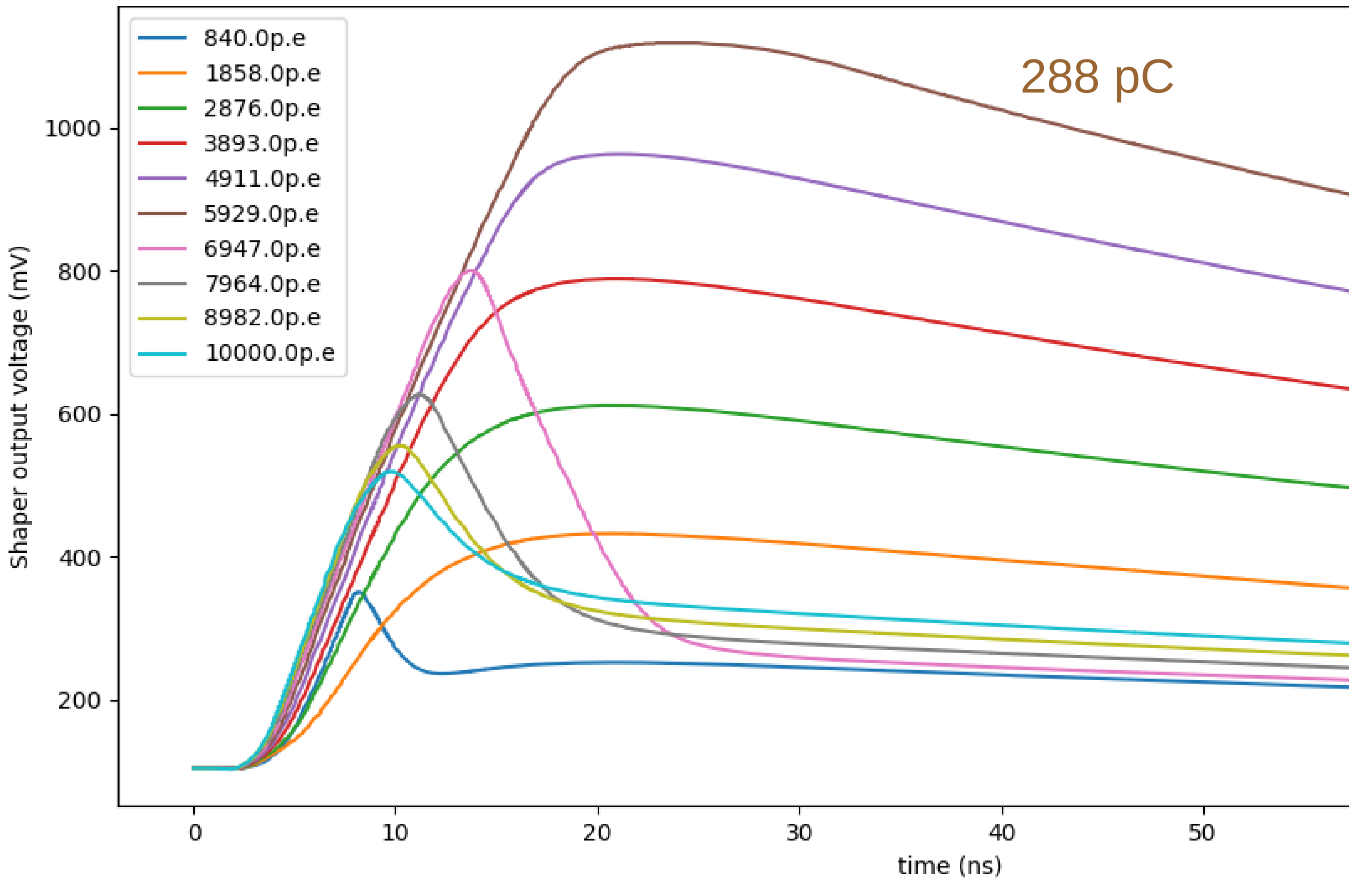
CALOROC1B: Charge and time simulations

- Waveform for HG on the left + gain switching on the right:
  - Example with C_{SiPM} of 10 nF
  - Gain of 1.8e5 electrons per p.e

Waveform for high gain shaper @ 10nF configuration

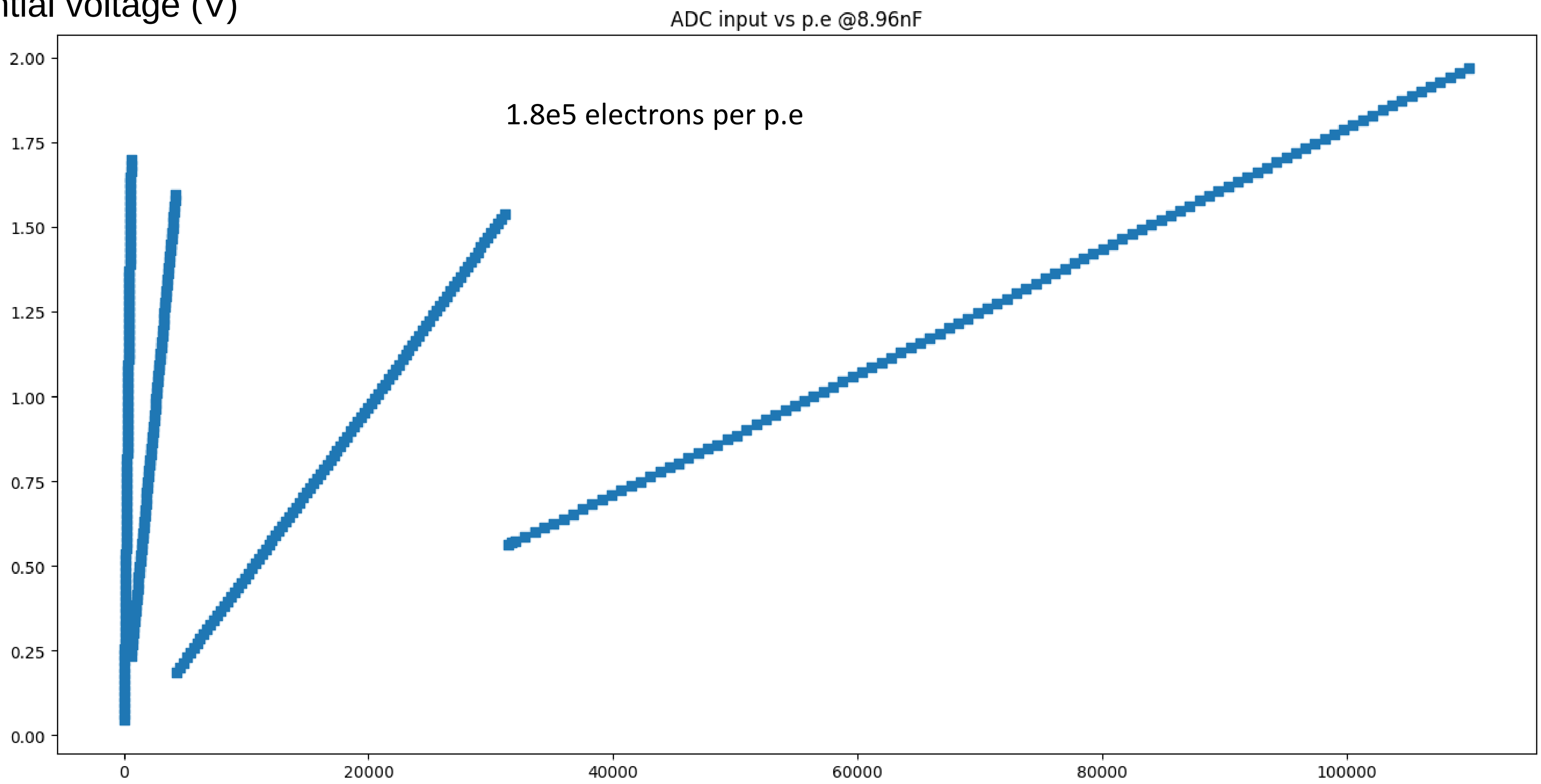


Waveform for medium gain shaper @ 10nF configuration



CALOROC1B: Linearity

Differential voltage (V)

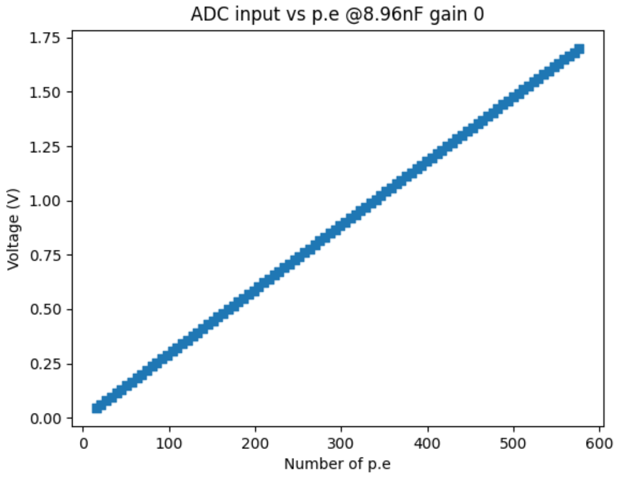


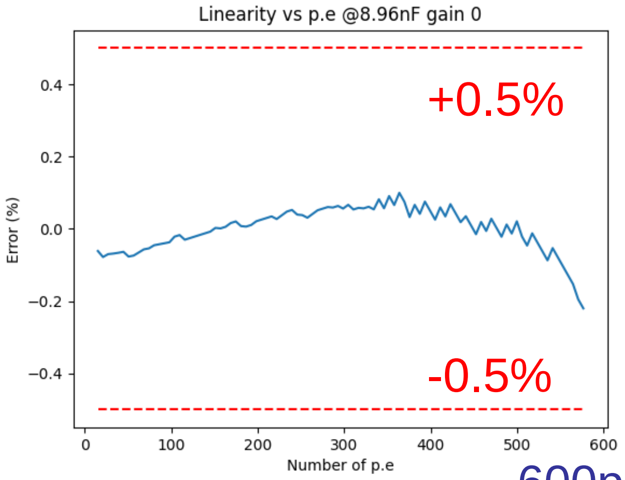
Number of photo-electrons (p.e)

110k p.e. = ~ 3 nC

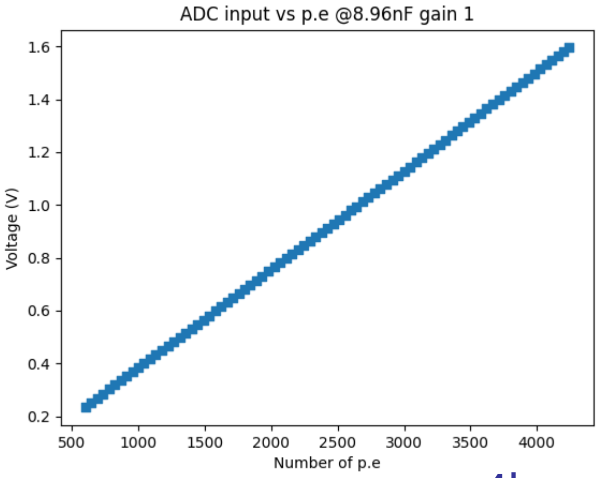
CALOROC1B: Linearity error

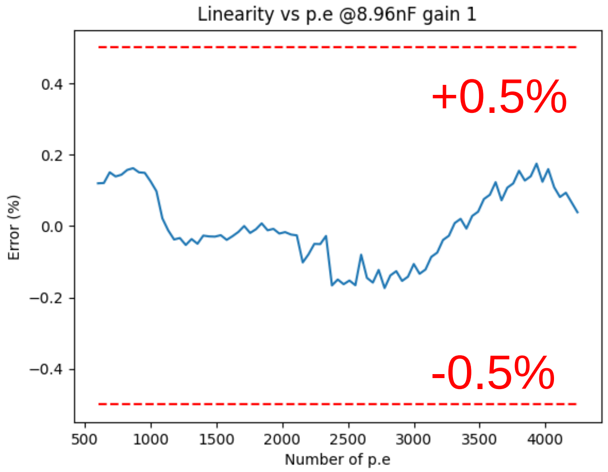
- Less than 1% linearity error
  - 1.8e5 electrons per p.e



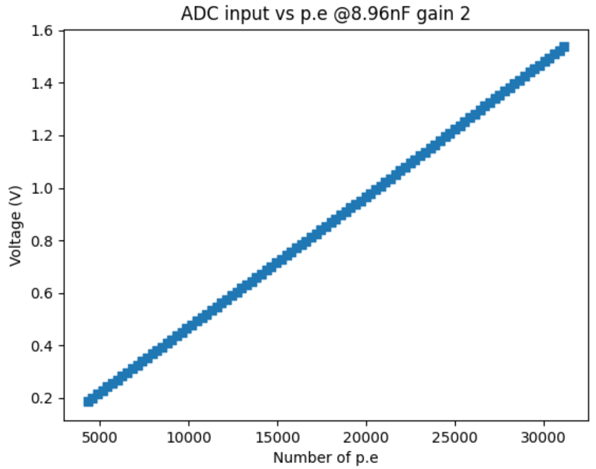


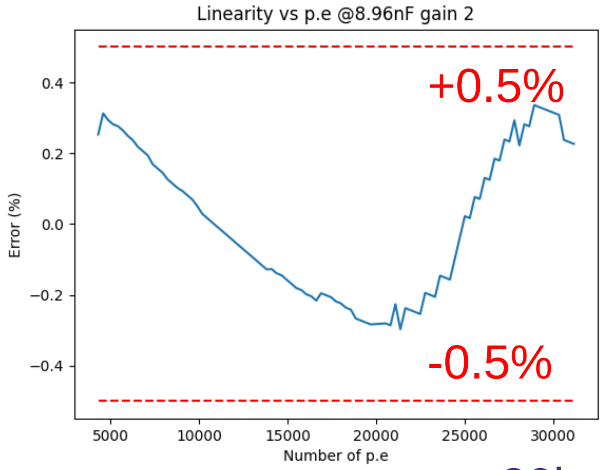
600p.e



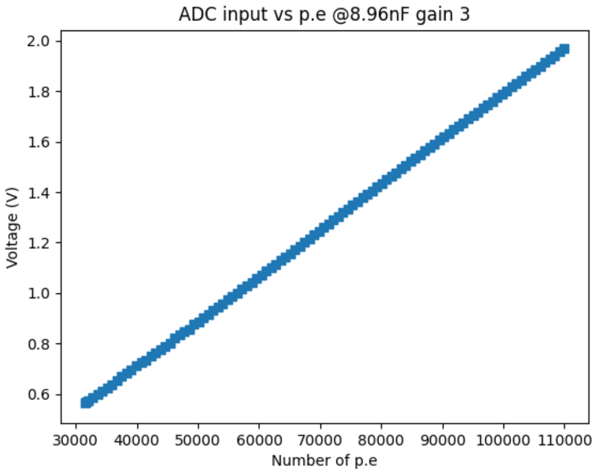


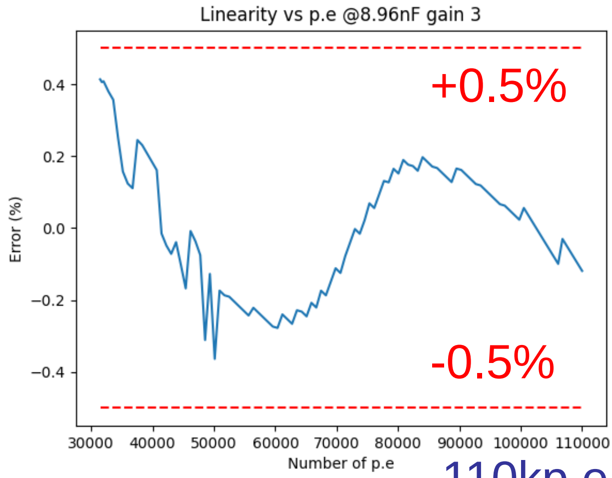
4kp.e





30kp.e

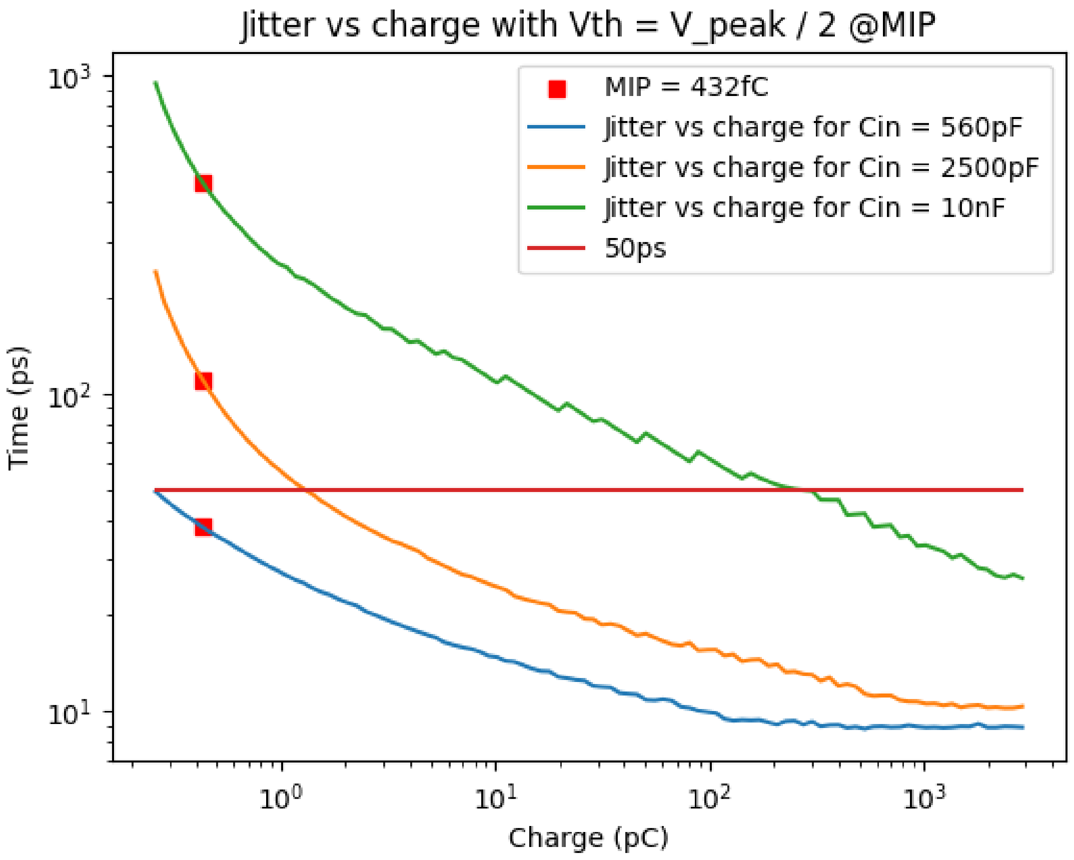


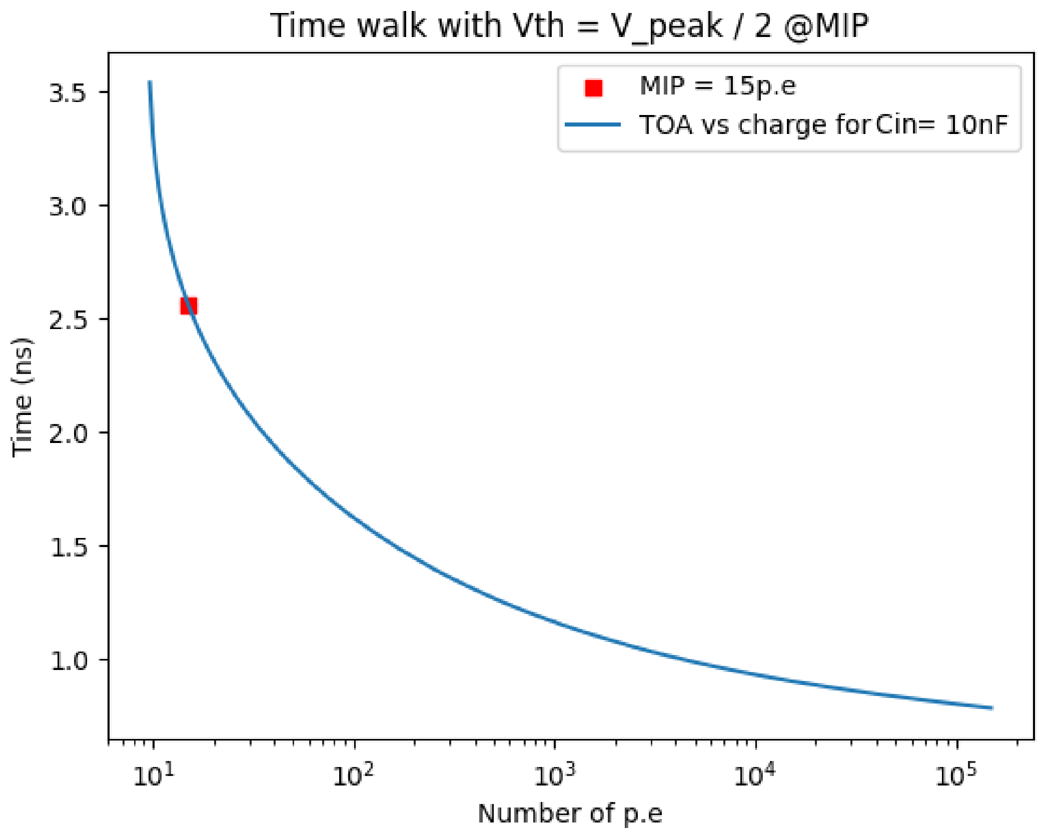


110kp.e

CALOROC1B: simulated timing accuracy

- Simulated time jitter remains below 50 ps with C_{SiPM} = 560pF
- Time walk is below ~2,5 ns with C_{SiPM} = 10nF, lower with smaller C_{SiPM}





CALOROC1B: simulated SNR vs SiPM size

© P. Dumas

- The SiPM configuration has a direct impact
  - **The full input dynamic range is limited by Q_{max}/C_{SiPM}**
  - SNR at 1 p.e. is proportional to Q/C_{SiPM}
  - Gain of 1.8e5 electrons per p.e (table below)

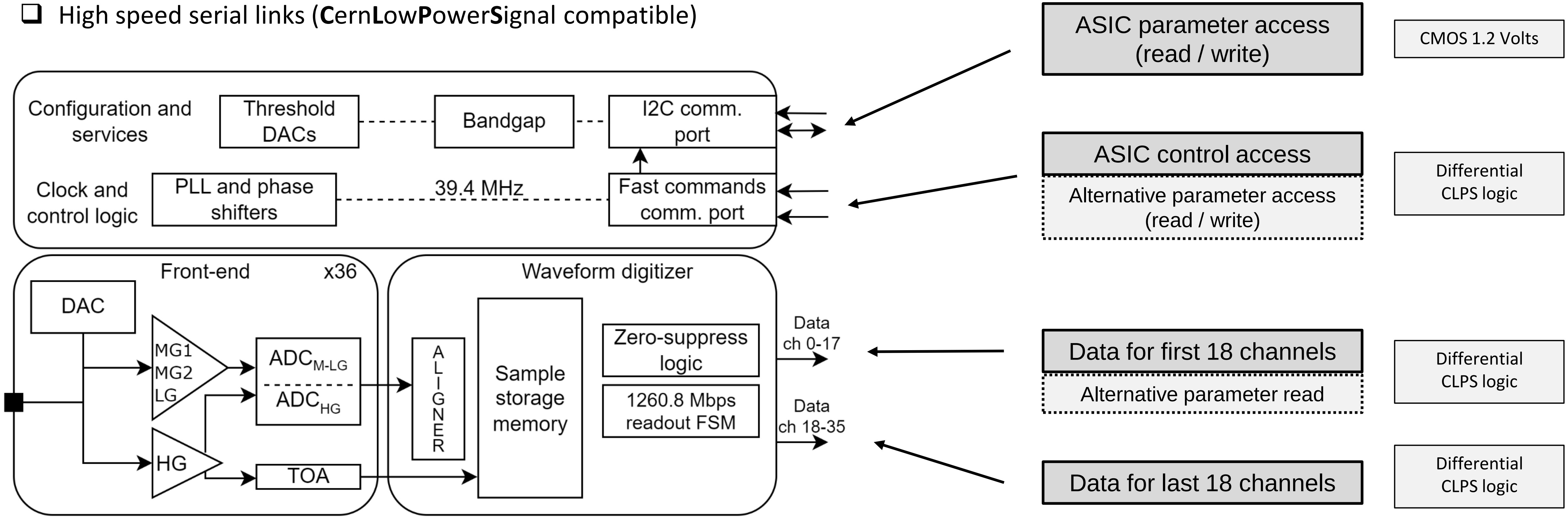
- CALOROC1b will be able to readout SiPM in the range ~ 500 pF to 10 nF
  - Timing measurements will focus on the MIP (~15pe)

Operation modes	1 SiPM of 530pF Caloroc1B	1 SiPM of 2.5nF Caloroc1B	4 SiPM of 2.5nF Caloroc1B	1 SiPM of 530pF Caloroc1A
Cin	530pF	2.5nF	10nF	530pF
Dynamic range in charge (Noise - Max)	2.6fC-190pC	12fC-770pC	48fC-3.1nC	20fC-320pC
Input time constant (occupancy related)	100ns	500ns	500ns	10ns
Jitter @ MIP (≈400fC)	35ps	110ps	470ps	400ps
SNR @ 1p.e (≈30fC@gain=1.8e5)	10	2.4	0.6	1.44

SiPM: S14160-3010PS 3x3mm (530pF) / S14160-6010PS 6x6mm (2.5nF)

CALOROC: Block Diagram – Interfaces [F. Dulucq]

- CALOROCs will have the same interfaces (comparable to CMS ones):
  - 1 clock @ 320 MHz + 2 resets (hard + soft)
  - Fast command to dynamically control the ASIC (differential)
  - I2C to set the parameters
  - High speed serial links (**C**ern**L**ow**P**ower**S**ignal compatible)



CALOROC: Fast Commands

- Commands to interact dynamically with the ASIC
  - 8 bits commands synchronized with incoming 320 MHz clock – MSB first
  - Only idle needed – others have a known latency
  - Detailed in the datasheet

Fast commands	Value	Description
Idle	00110110	Default command inside
ChipSync	11010010	Reset FSM, buffers and counters
BCR	00011101	Reset timestamp counter to a default value
EBR	11010001	Empty readout buffers
PING	10011001	Ping status and counters
LinkResetROCD	10011010	Transmission of synchronization patterns
ROC-Serializer-Reset	10011100	Reset serializer link module only
L1A	01001011	External trigger (all channels)
CalPulseInt	00101101	800 ns internal calibration pulse
CalPulseExt	01111000	100 ns external calibration pulse
SC_0	01011010	I2C over fast command - send '0'
SC_1	01011100	I2C over fast command - send '1'
SC_Valid_Reset	10001011	Valid or reset (2 consecutives) current transaction

- Idle → Default command
- ChipSync, BCR, EBR, PING: Resets and synchronization
- LinkResetROCD, ROC-Serializer-Reset: Serial links recovery
- L1A, CalPulseInt, CalPulseExt: Calibration and pseudo-heartbeat
- SC_0, SC_1, SC_Valid_Reset: Slow control (I2C) over fast commands

CALOROC: Readout Frames

- For charge measurements, CALOROC-A based on ADC/TOT, CALOROC-B only ADCs

CALOROCA (CMS-like)

4b-data Header	2b Mode	Dh Ts	1 - 6b evt counter - 0 - 16b Timestamp	1

4b-hit Header	8b 0	Dh Hm	Dh Ch	18 channels Hit map

Tc	Tp	10b ADC-1	10b ADC or TOT (Tc = 1)	10b TOA
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA
⋮				
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA

CRC

Idle/Sync Header	28b default IDLE Pattern

CALOROCB – 2 ADCs or 1 ADC (4 gains)

4b-data Header	2b Mode	Dh Ts	1 - 6b evt counter - 0 - 16b Timestamp	1

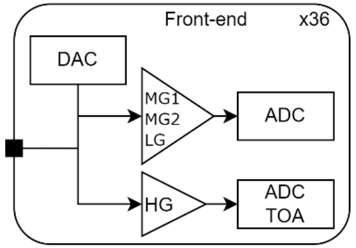
4b-hit Header	8b 0	Dh Hm	Dh Ch	18 channels Hit map

2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA
⋮			
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA

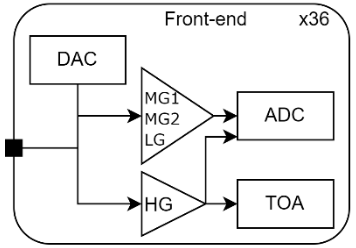
CRC

Idle/Sync Header	28b default IDLE Pattern

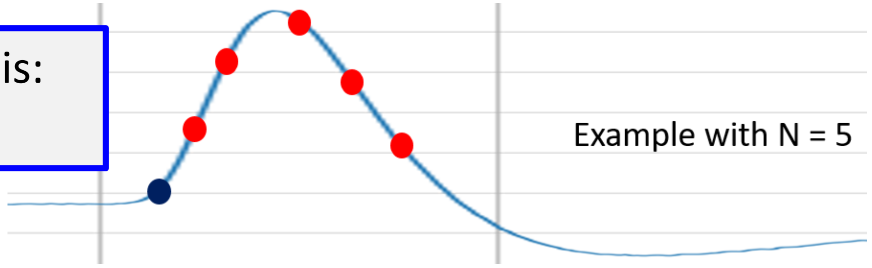
CALOROCB (2 ADCs)



CALOROCB (1 ADCs)



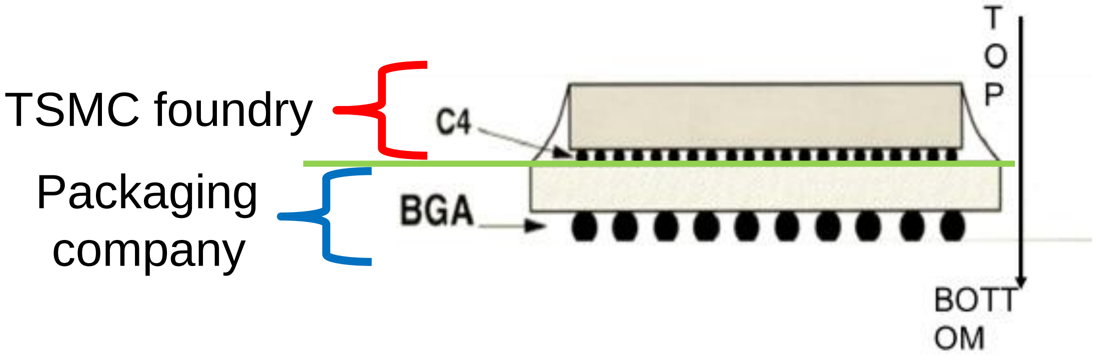
In ZS mode, for **X** (1-18) hit channels and **N** samples, number of 32-bit words is:
N x (2Headers + **X** + 2Trailers)



In characterization mode, forced TcTp, ADC, TOT, TOA for all channels

CALOROC Packaging

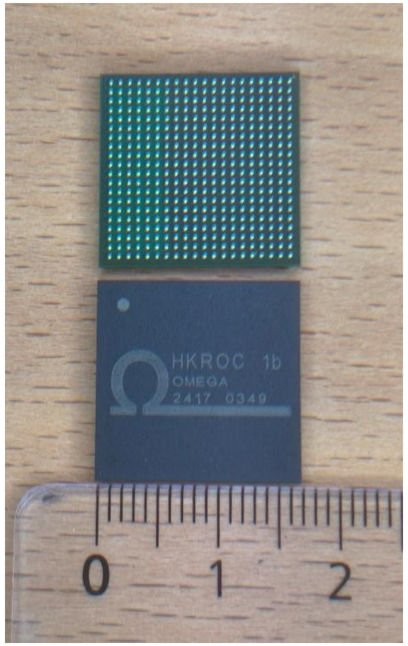
- CALOROC will have the same package as the existing HKROC:
  - JEDEC MO-216 – 17 x 17 mm BGA version
  - 400 balls with 0.8 mm pitch
  - Specific substrate (interposer) designed at OMEGA
  - **QR code** like HGCROC3



JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: THIN PROFILE, SQUARE AND RECTANGULAR, BALL GRID ARRAY FAMILY, 1.00 & 0.80 mm PITCHES	ISSUE: E	DATE: AUG 2003	MO-216

TABLE 3: SQUARE VARIATIONS – 0.80 PITCH

D / E	e = 0.80							
	MD/ME	N	SD/SE	VARIATION	MD-1/ME-1	N	SD/SE	VARIATION
14.00	17	289	0.00	BAJ-1	16	256	0.40	BAJ-2
15.00	18	324	0.40	BAK-1	17	289	0.00	BAK-2
16.00	19	361	0.00	BAL-1	18	324	0.40	BAL-2
17.00	20	400	0.40	BAM-1	19	361	0.00	BAM-2

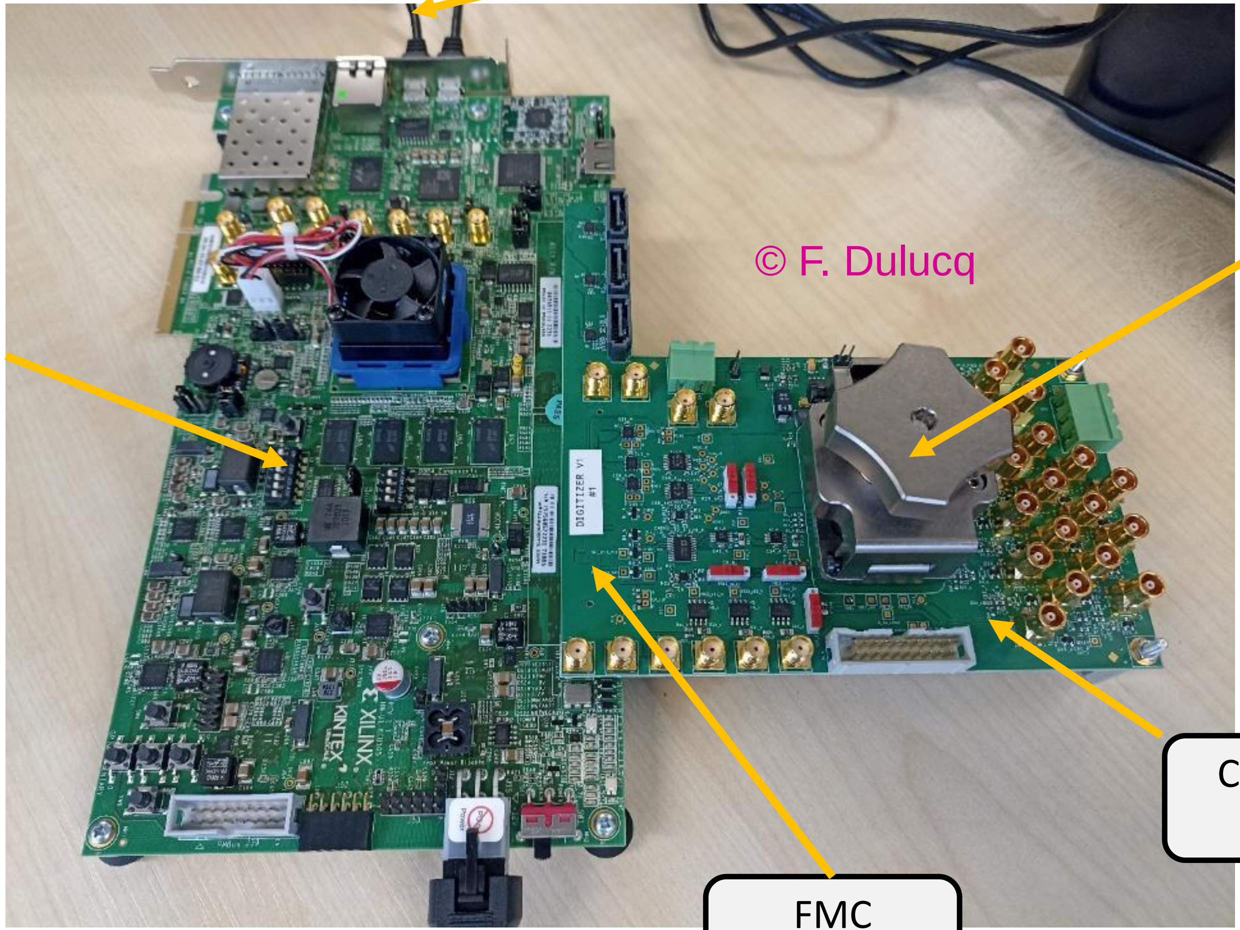


Test System for Characterization

- CALOROC characterization motherboard under design at OMEGA:
  - Originally developed for HGCROC and HKROC
  - Well-known at OMEGA and LLR (firmware based only)
  - Compatible with KRIA motherboard (CERN) but software + firmware needed

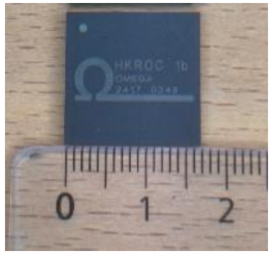
Python scripts

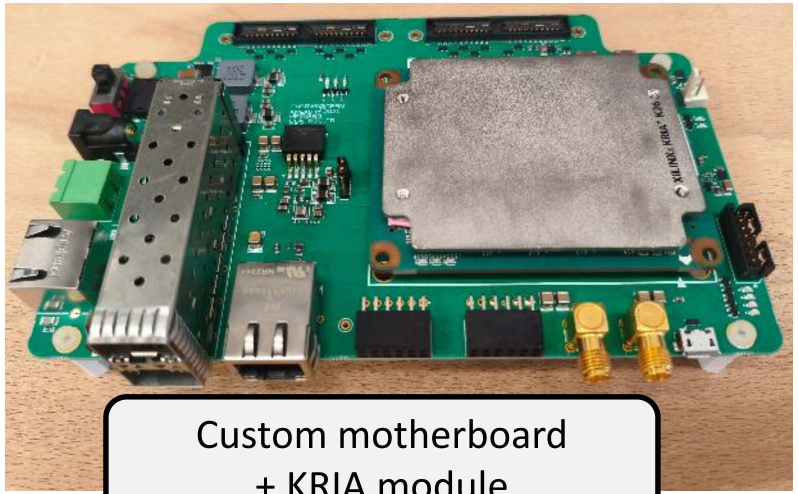
Monitor Program Test



Commercial KCU105 board

CALOROC BGA socket





Custom motherboard + KRIA module

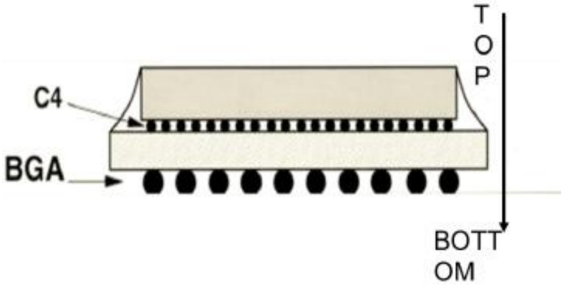
FMC connector

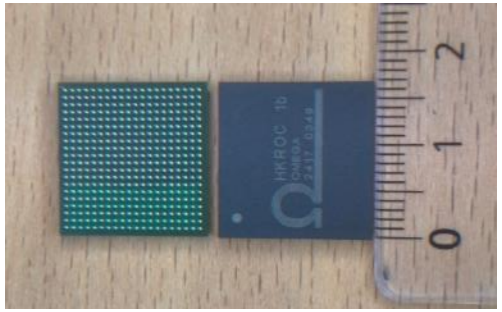
Custom CALOROC motherboard

Conclusion

- CALOROCs first prototypes for EIC
  - 1A/1B for SiPM readout
  - 36 channels for charge and time measurement
    - ADC + ToT or ADCs only with gain-switching
  - Waveform digitizer up to 7 samples
  - Streaming readout
  - Rate limited by output serial links

- Fabrication
  - Engineering run submitted in september, received at Xmas
  - BGA packaging in February 2026
  - Expected first samples in March





CALOROC1B: Dynamic range and resolution

- The SiPM configuration has a direct impact on the dynamic range
  - The highest measurable charge is determined by the SiPM input capacitance.
  - The ratio between the highest and the lowest measurable charge is constant (dynamic range ratio).

- 10b resolution and 17b dynamic range
  - With a 10b ADC and 4 gains (2b) we have a resolution of 17b
  - The measured charge is in the format of $10b \, * GainRatio^{2b}$
  - The gain ratio can be adjusted to increase the dynamic range in exchange for a lower resolution.
  - Using the highest resolution the dynamic range ratio is 70k
  - Supposing 1MeV = 1p.e for the 8.96nF setup this should give us a dynamic range of 1.5MeV (noise floor) to 110GeV