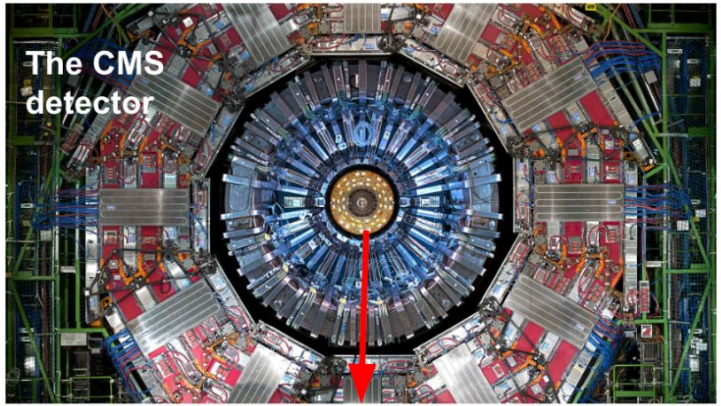
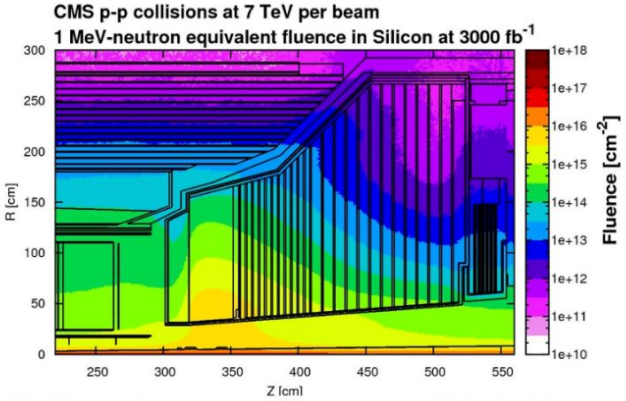
Performance of a charge injection board

Jasmine Chhikara, Rajdeep Mohan Chatterjee, Shilpi Jain, Gobinda Majumder, Mandar N. Saraf

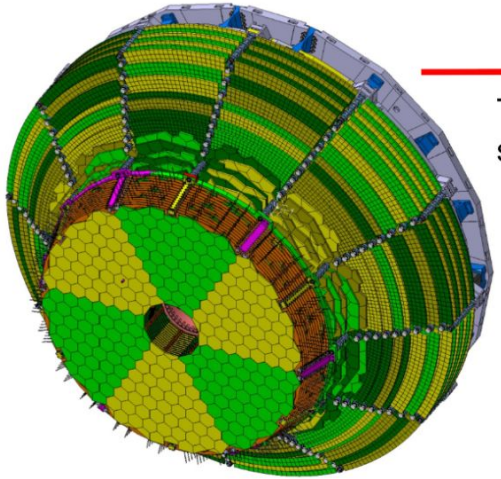
Motivation



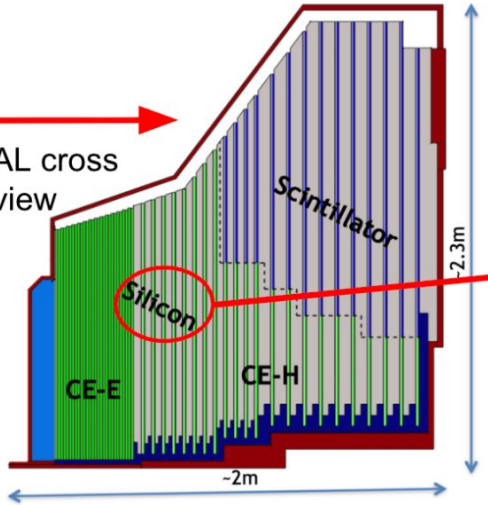
HL LHC→ increased pileup and radiation damage

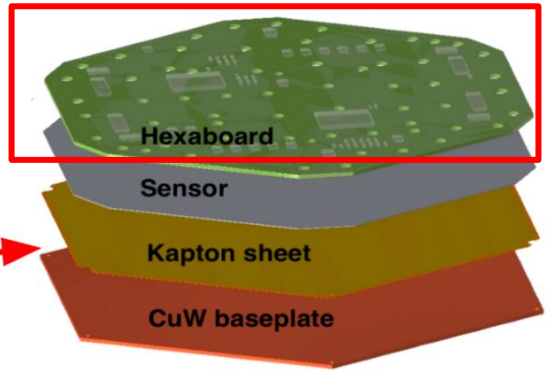


Upgrade endcap to HGCAL



The HGCAL cross sectional view

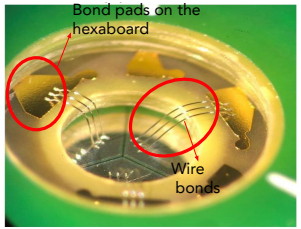


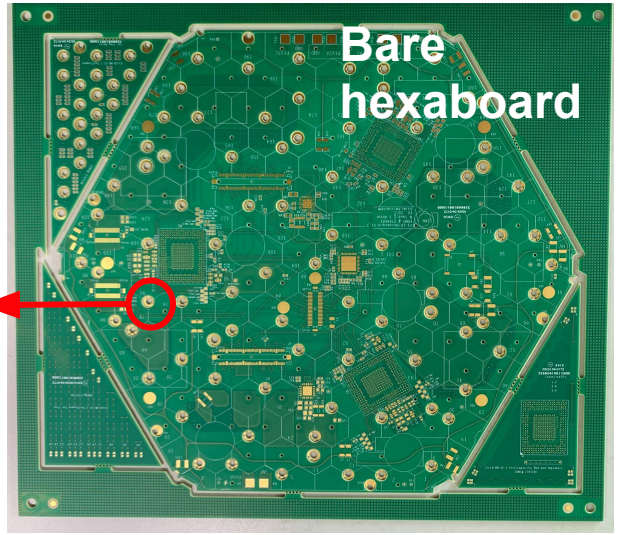


A Silicon based module

Hexaboard, its assembly and features (HGCROC)

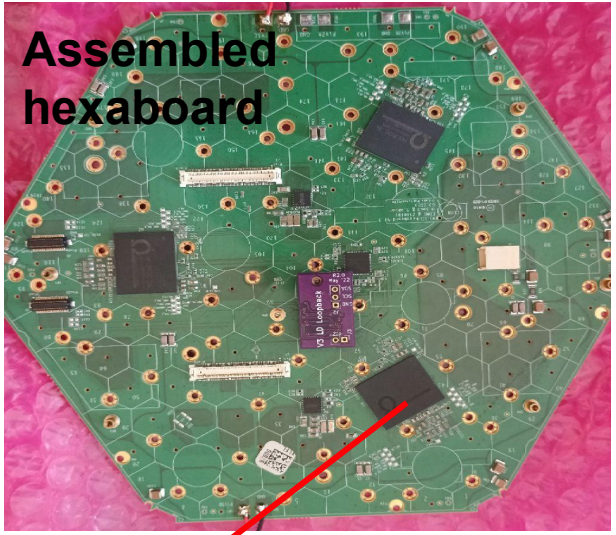
8 layered PCB
Stepped hole structure.

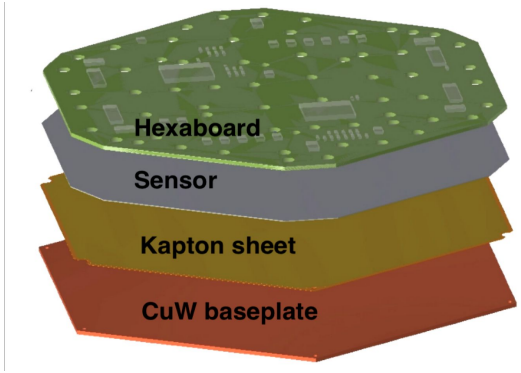




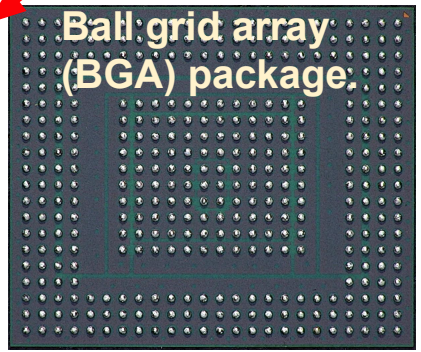
ROCs, connectors, LDOs, rafael

Depanel



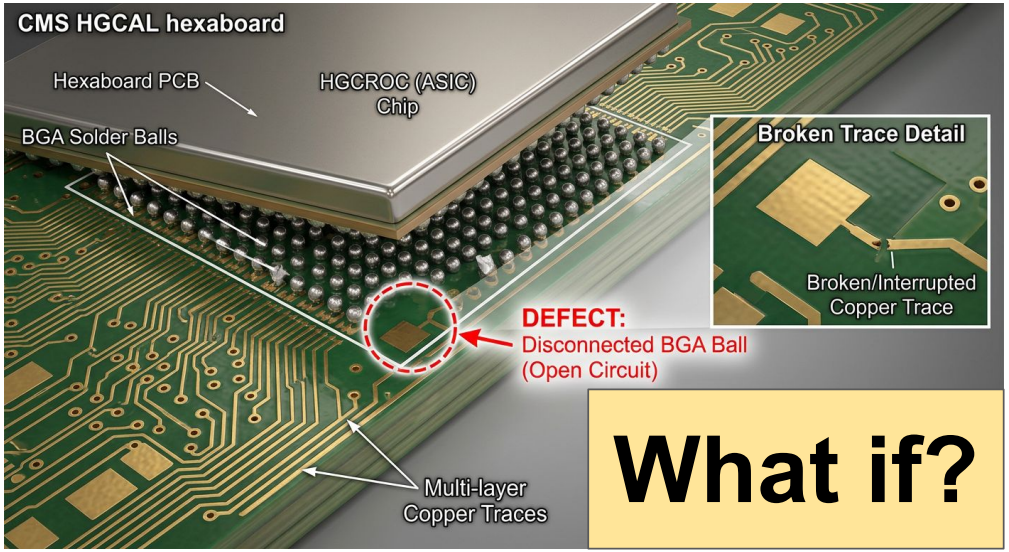


- Wire bond from silicon sensor to gold bond pads on 6th layer of assembled hexaboard (**HB**).
- Signal from bond pads to ASIC via traces



Need for a non - invasive testing method

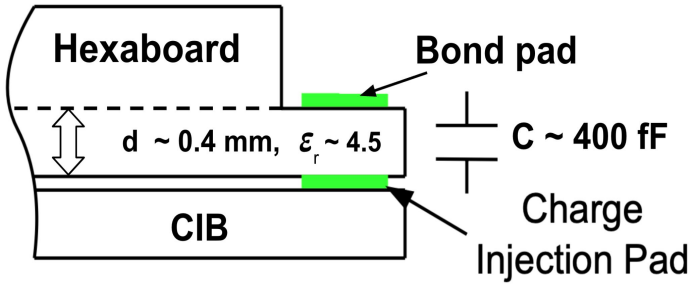
- Disruption in connectivity due to incomplete or faulty BGA solder joints or Broken or damaged PCB traces.
- Such failures result in dead or inefficient readout channels.



- The detector will sit there for ~ 15 years.
- Therefore, verifying connectivity and functionality of every HGCROC channel is essential

A **non-invasive testing method** is required, as the gold hexaboard bond pads are extremely fragile.

- ~400 fF Q_{inj} capacitor
- Pulse generator:
  - 0.2-15V step
  - 80fC → 5.8pC



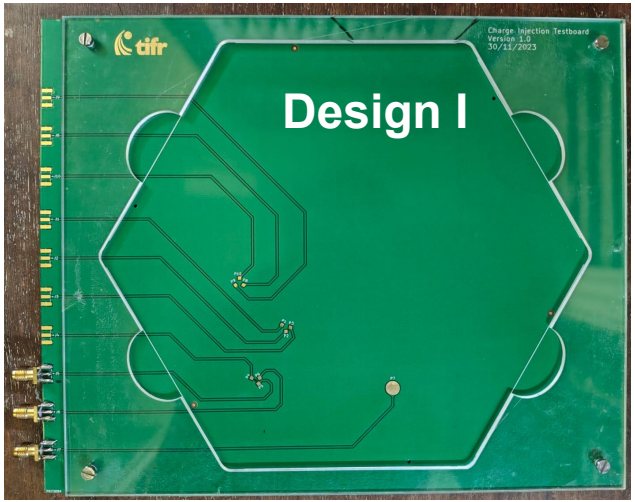
Capacitive coupling

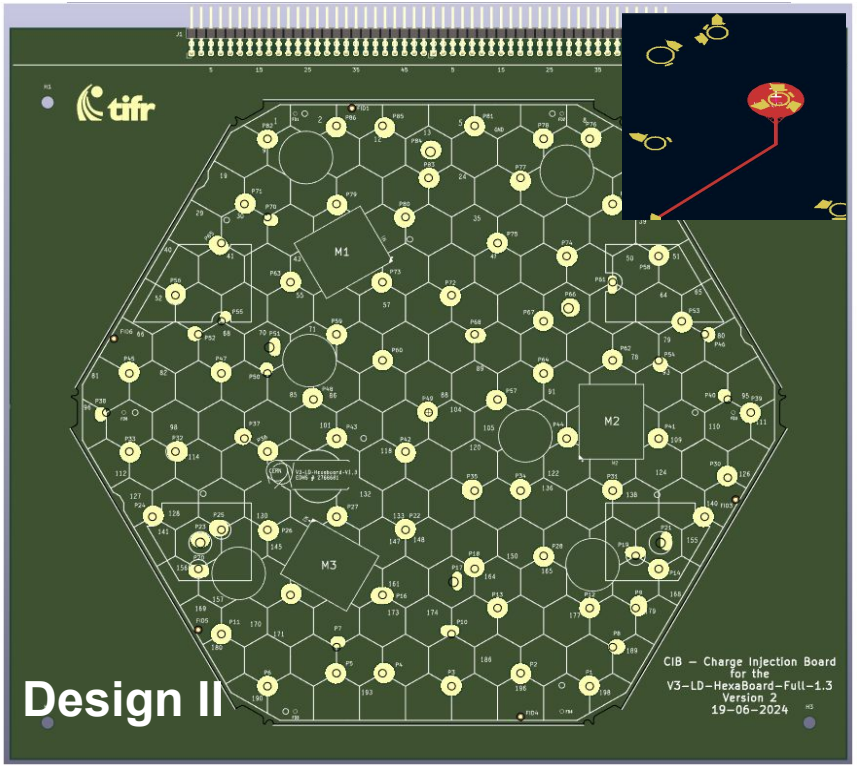
Building blocks of charge injection system: (1) charge injection board

Details already covered in Mandar N. Saraf's talk

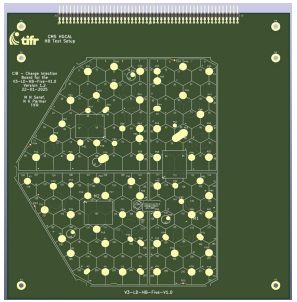
Design I: Have 1 injection pad cover 1 HB bond pad

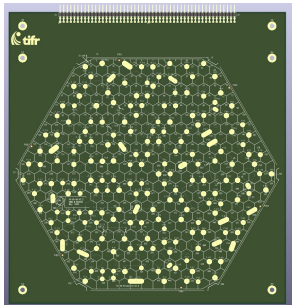
Design II: Have 1 injection pad cover 1 stepped hole of HB i.e., 2 or 3 silicon channels





Charge injection board for different variant of HB



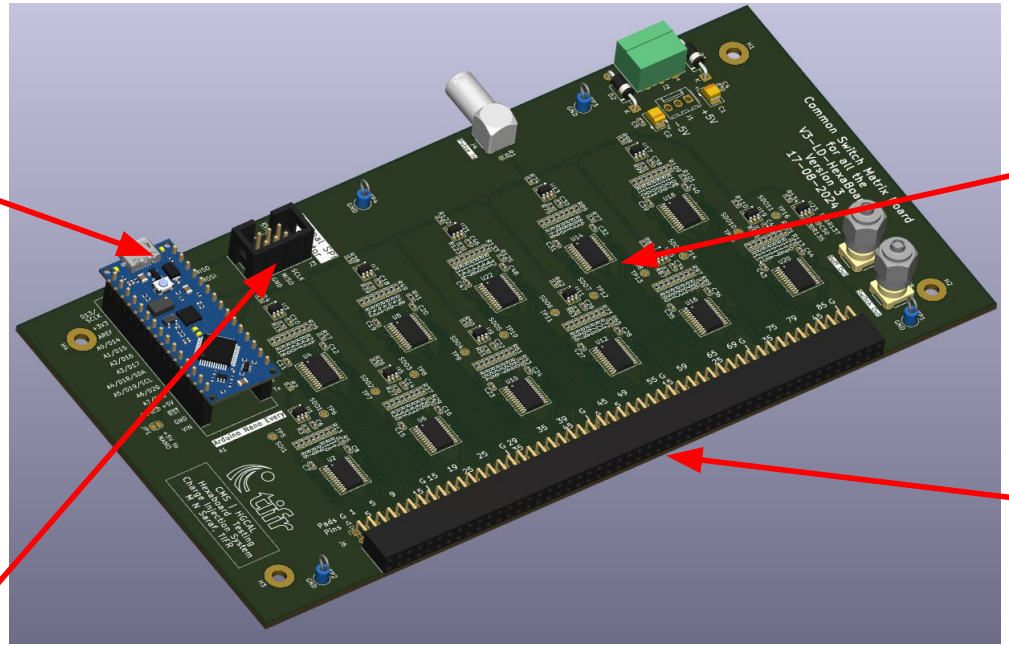


Building blocks of charge injection system: (2) switch matrix

Details already covered in Mandar N. Saraf's talk

Arduino for controlling channels

Multiplexed system: master controller



ADG 1414: analog switches 8 channels per chip

Connection to charge injection board

Test setup

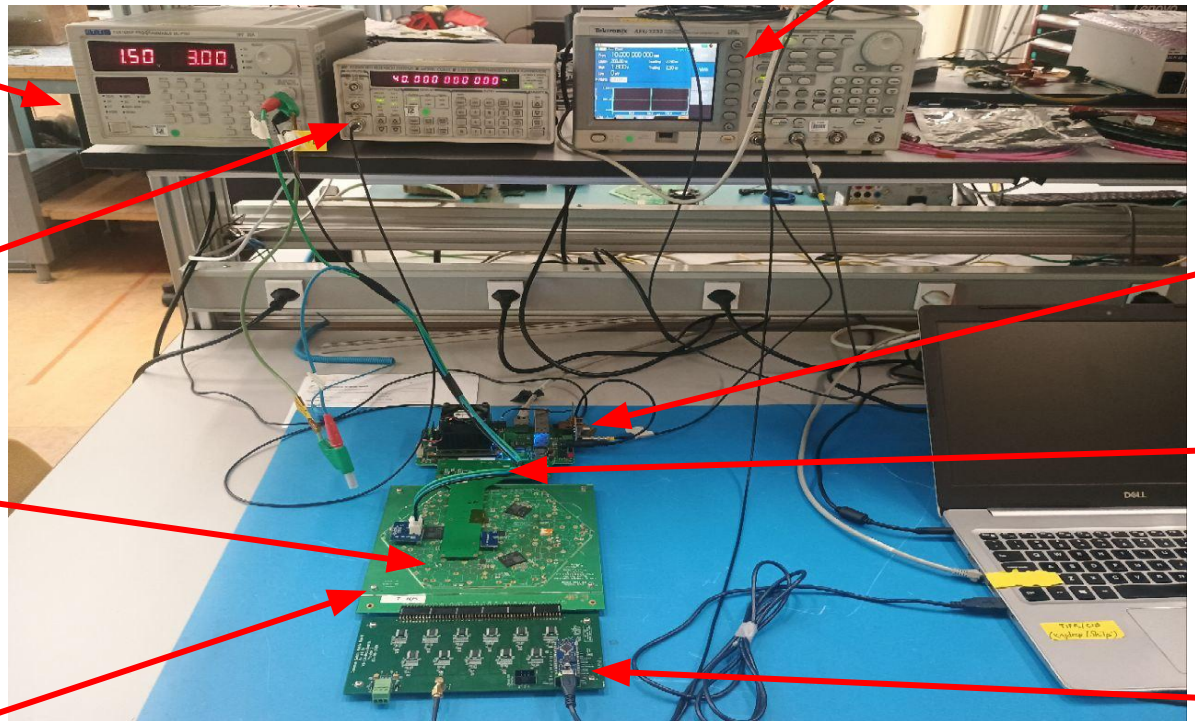
Dual channel function generator:
Source for:
Ch1 - Charge injection pulse
Ch2 - Synchronous trigger pulse

Input supply of 1.5 V to hexaboard analog and digital parts

SRS clock generator 40 MHz LVCMOS1.8 clk

Hexaboard Low density (LD)

Charge injection board (CIB)



Kria SOM based Hexacontroller Furbished with Heatsink and Fan

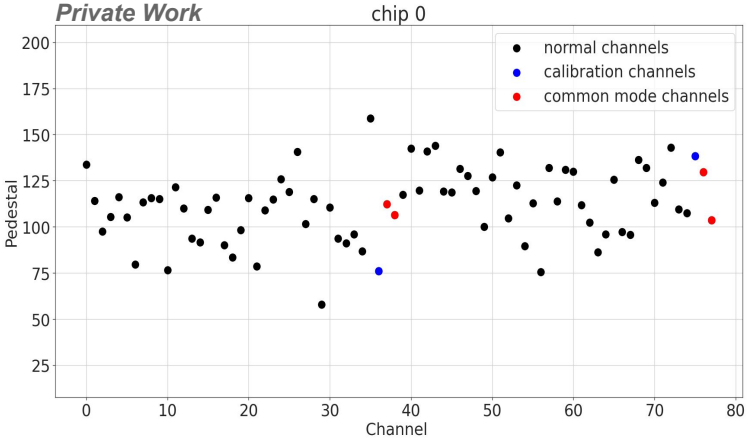
Trophy LD

Switch matrix Board:
1:86 Fanout and Switch On/Off

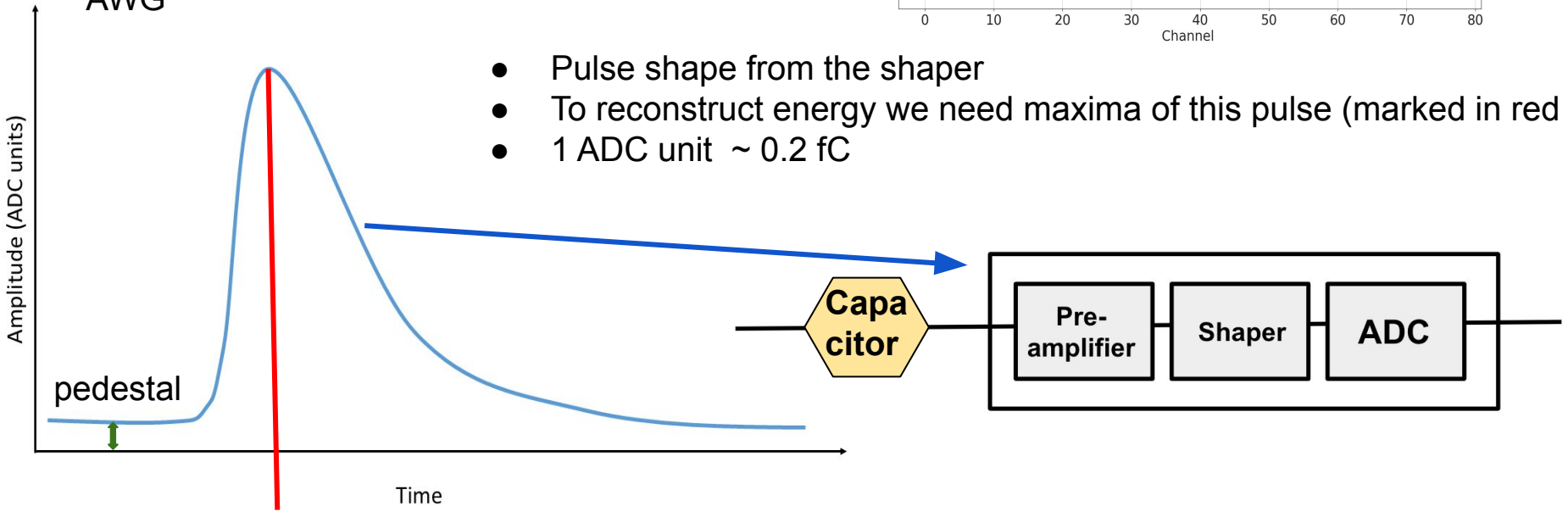
Methodology for testing the concept of capacitive coupling

Pulse shape

- Pedestal : the ADC value associated with the baseline level of the analog signal when there is no actual signal or input present
- Keeping the injection and trigger pulse off from AWG

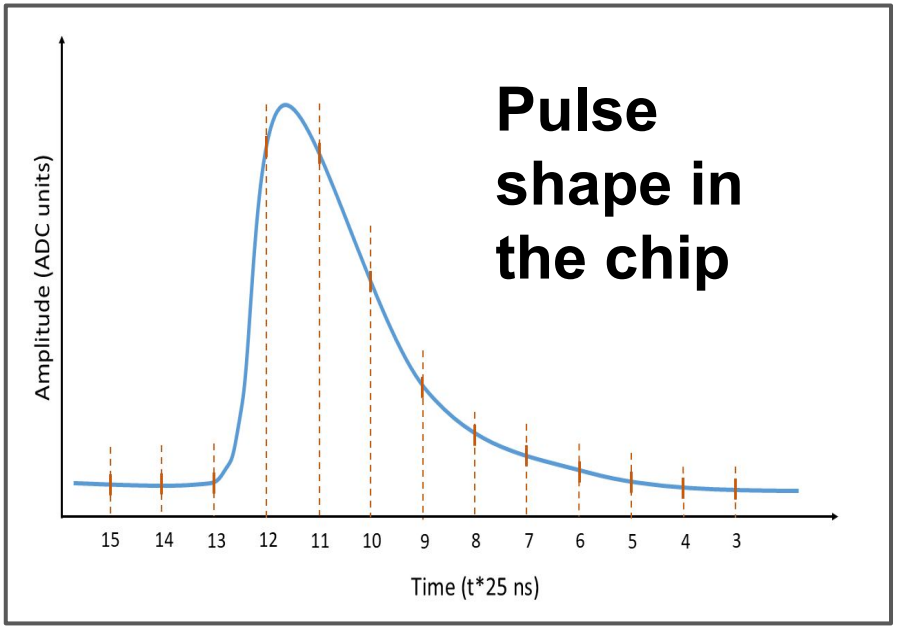


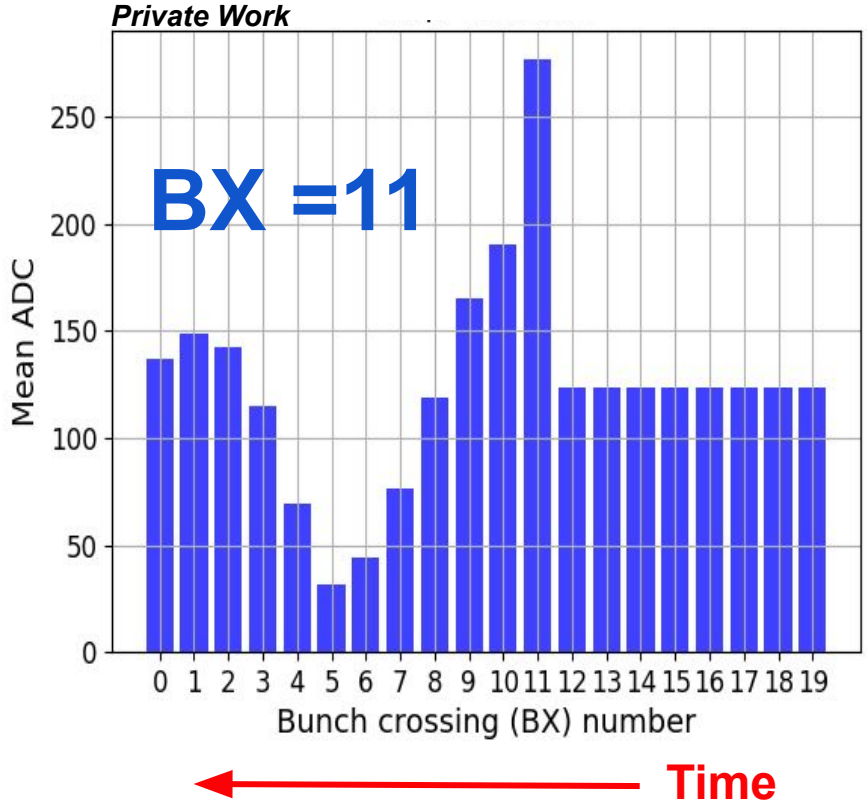
- Pulse shape from the shaper
- To reconstruct energy we need maxima of this pulse (marked in red)
- 1 ADC unit ~ 0.2 fC



Finding out the best 25 ns window - I

- To know the best **25 ns window** (**hereby referred to as 1 bunch crossing or BX**) of maximum response i.e., maximum mean ADC value.

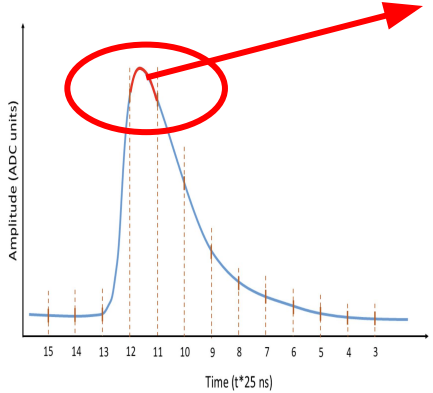


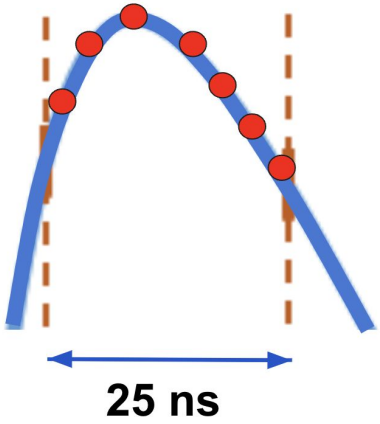


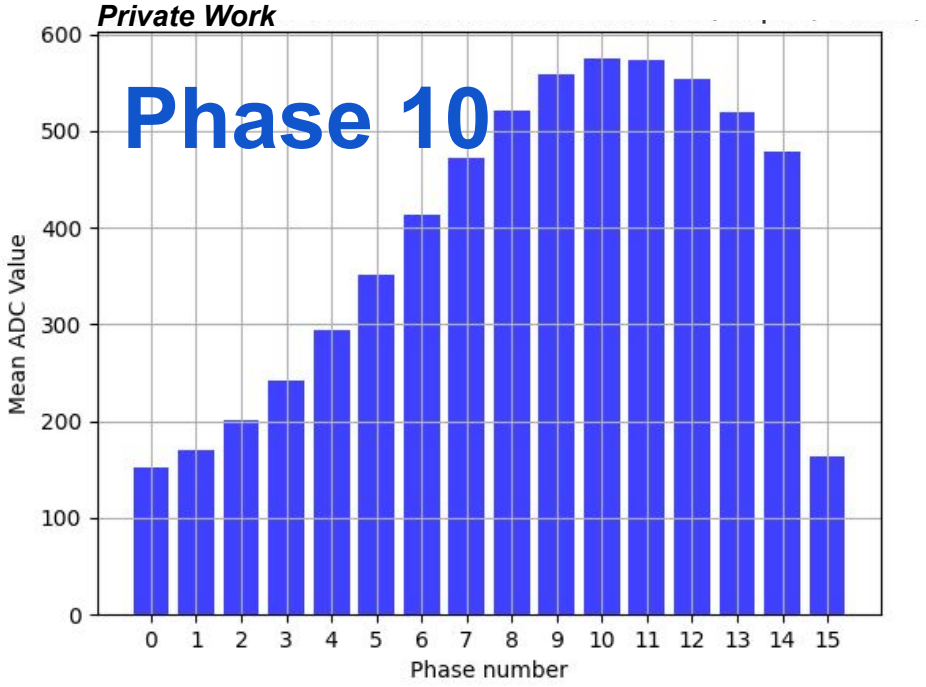
Which instant in the best chosen 25 ns window - II

- To know the phase (within BX = 25 ns) of maximum response i.e., maximum mean ADC value.

Divide the 25 ns within 16 more points





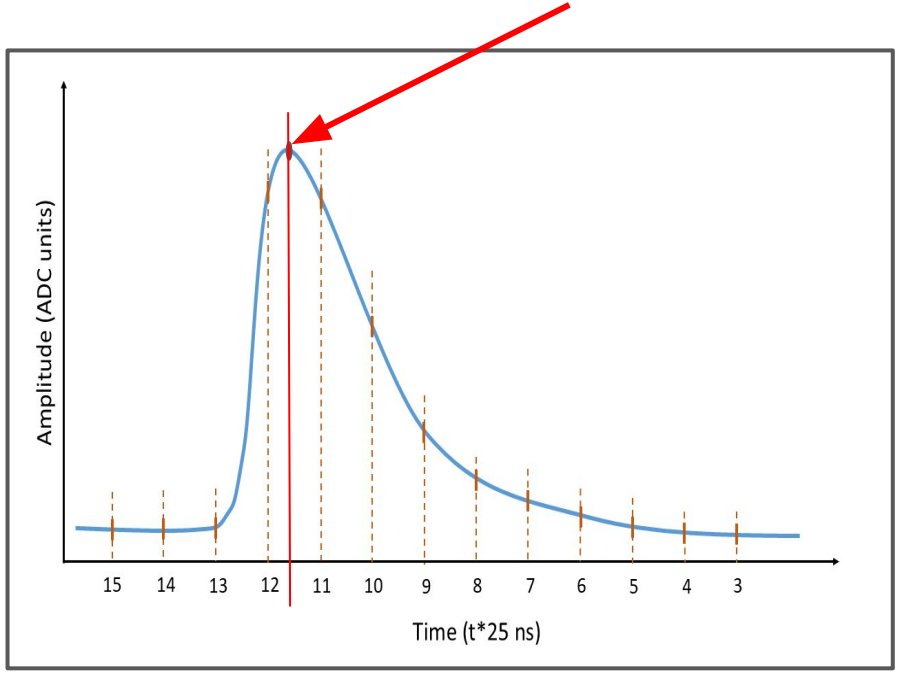


In BX = 11

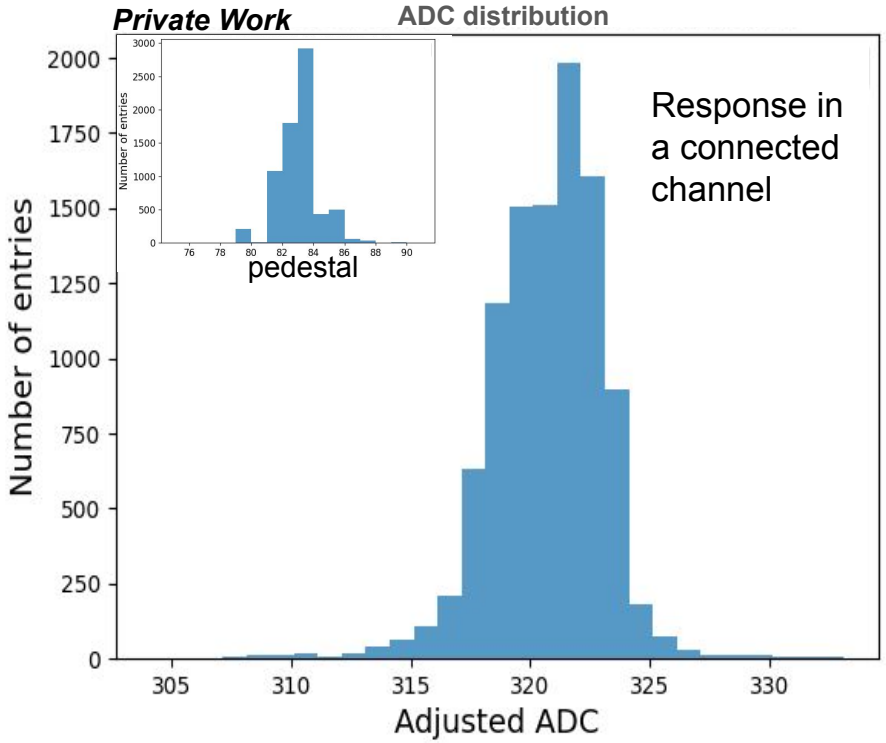
Time

Performance Test : External charge injection Run - III

- To get the peak of the pulse ask system to give ADC value after delay corresponding to BX=11 and phase=10



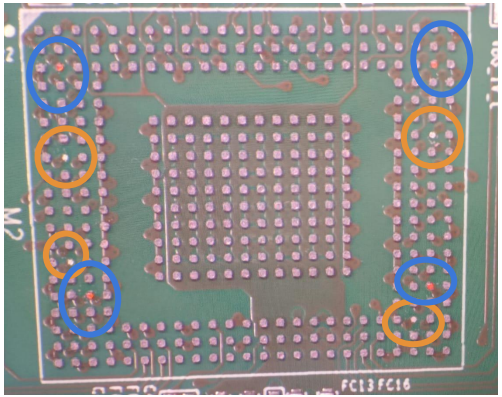
Adjusted = External injection ADC - mean pedestal



Test the concept with real bad channels

- Thorough inspection of the board for the presence of any non-working channels.
- External injection: few channels were not responsive.
- To further validate the method, channel failures were intentionally introduced

Blue: Method 1
Orange: Method 2

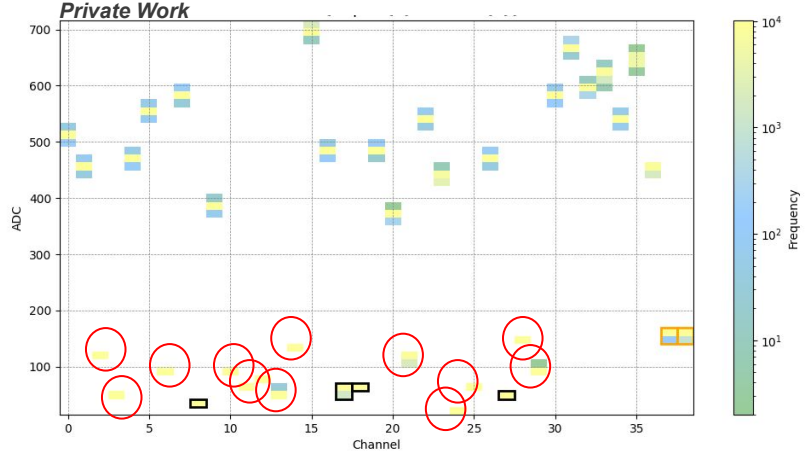


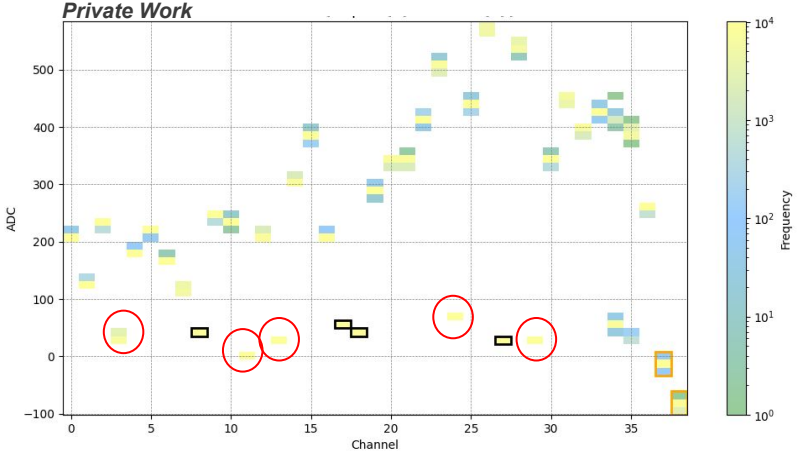
Method I: **Solder masking method**: A mask was placed between the BGA ball and the corresponding hexaboard PCB pad.
Method II: **Ball removal method**: The BGA ball corresponding to a specific channel was physically removed

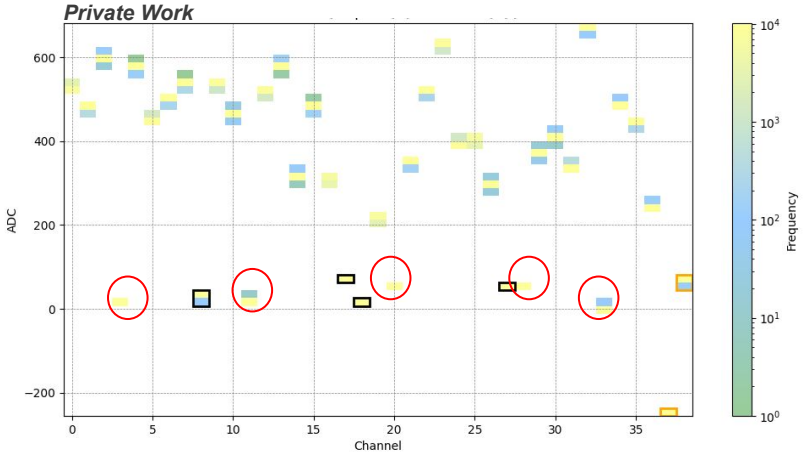
To prove the functionality of the Charge injection system, blinded analysis performed by reworking 16 channels across 2 ASICs by above method.

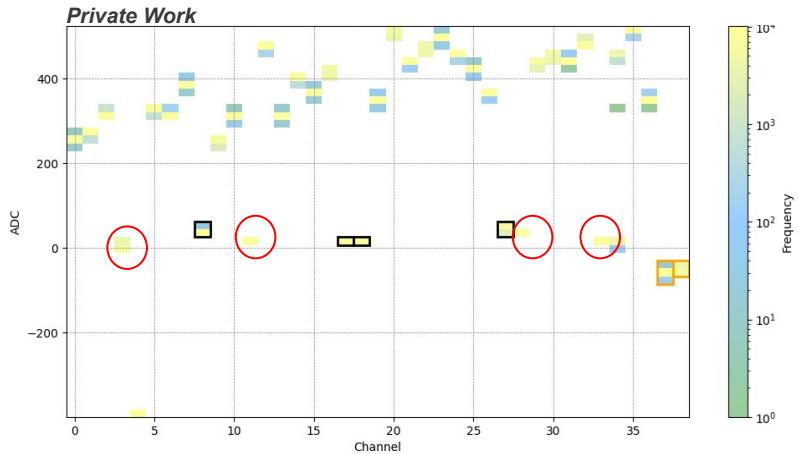
Tests after chip rework

External injection: Pedestal subtracted ADC values at 1V below threshold of (ADC-pedestal = 100)





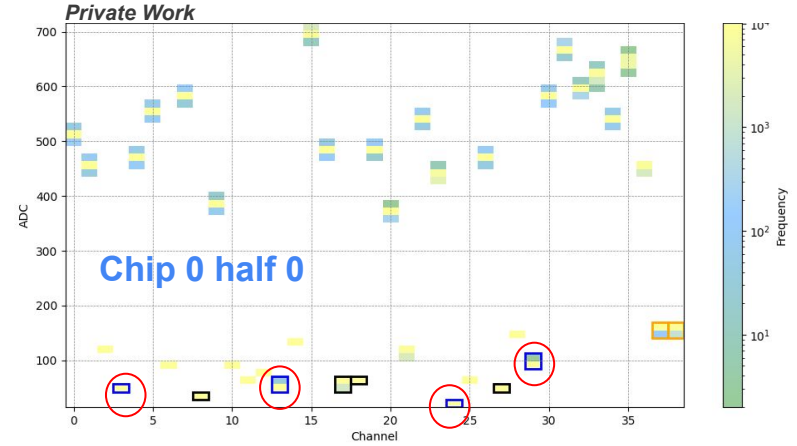


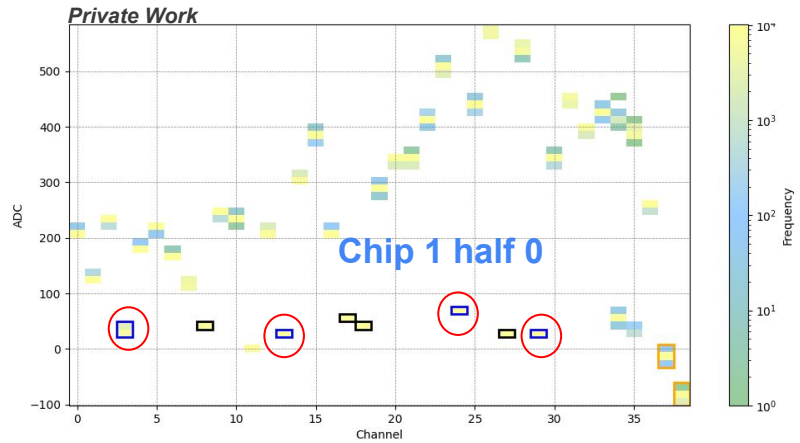


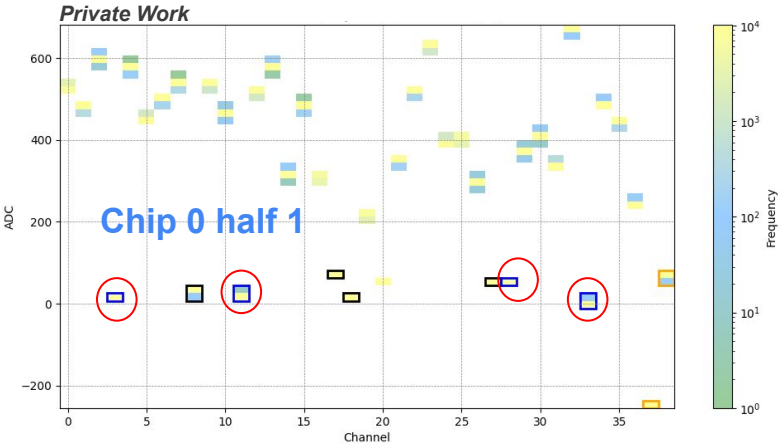
Results after unblinding

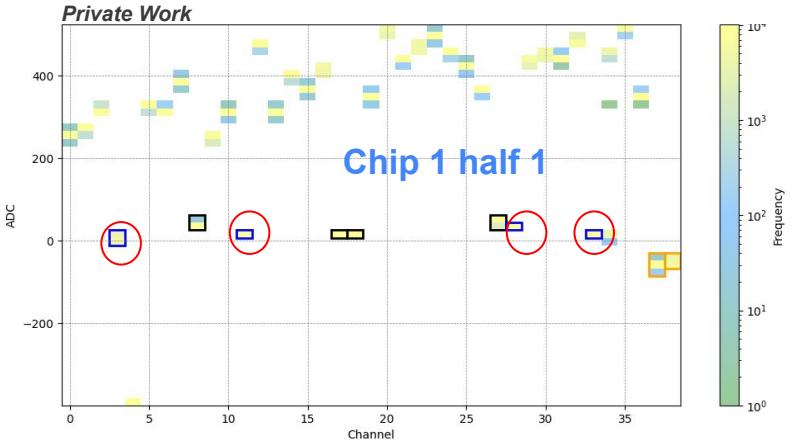
External injection: Pedestal subtracted ADC values

All the 16 channels marked in red circles can be seen to have low ADC values i.e., no response to external injection









Summary and outlook

- Charge Injection System: Detects bad channels, not possible to detect with pedestal and noise level measurements.
- Setup at CERN:
  - The setup at CERN was used to test approximately 600 hexaboards.
  - Non-functional channels were observed across multiple boards.
  - These non functional channels could be identified with this setup which was not possible with any other non invasive electrical test.
  - Efficiency: 100% detection rate for channels with no connectivity and 0% false positive rate.
- The charge injection system is now operational at various labs (at TIFR, CERN, University of Alabama) and one production company (Merritronix (hyderabad)). The work and results have been presented in collaboration.
- The setup has been **successful in detecting the unconnected channels**
- The setup is now part of official quality control (QC) tests of hexaboards.
- Future Use: Plans to extend for studying timing and crosstalk among channels.

Backup

Blinded analysis

- A blinded analysis was performed to avoid bias in the validation.
- The identities of the intentionally faulty channels were not disclosed.
- Based solely on the charge injection response, the following channels were identified as non-functional:
  - Chip 0: 2, 3, 6, 10, 11, 12, 13, 14, 21, 24, 25, 29, 42(39), 50(47), 59(56), 67(63), 72(69)
  - Chip 1: 81(3), 91(13), 102(25), 107(29), 120(39), 128(47), 145(63), 150(69)
  - Chip 2: 196 (37)

(Bracket : local chip ID)

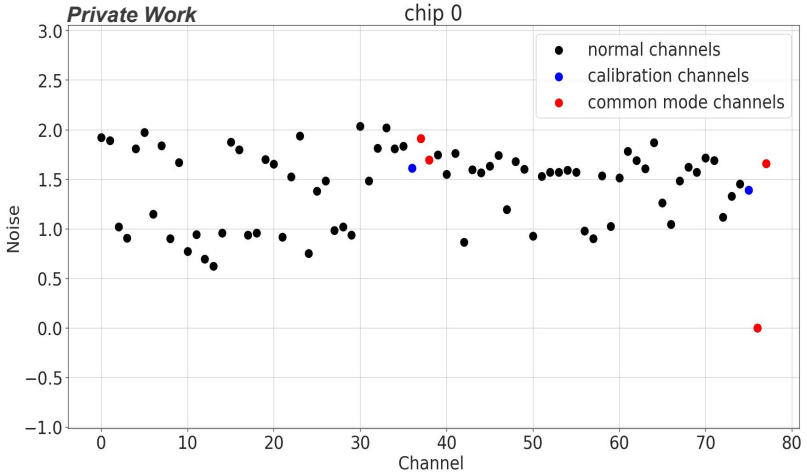
After unblinding, the list of channels below are the ones that were intentionally made bad.

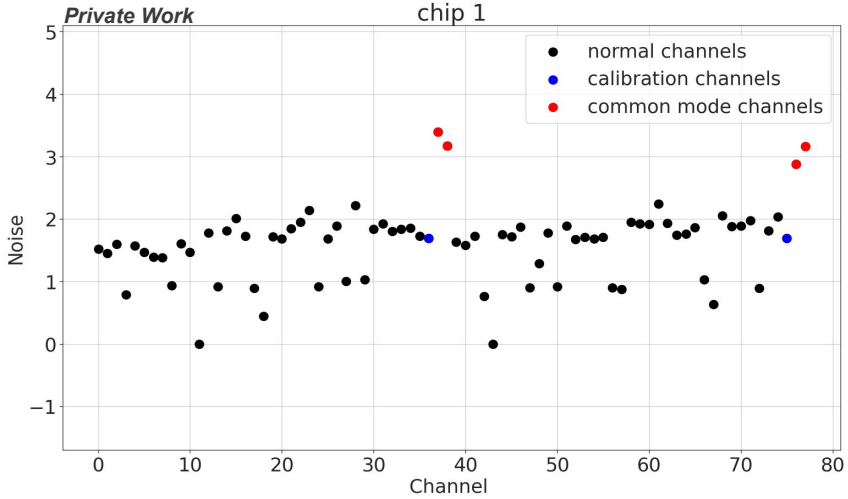
- **Chip 0: 3, 13, 24, 29, 42(39), 50(47), 67(63), 72(69)**
- **Chip 1: 81(3), 91(13), 102(25), 107(29), 120(39), 128(47), 145(63), 150(69)**

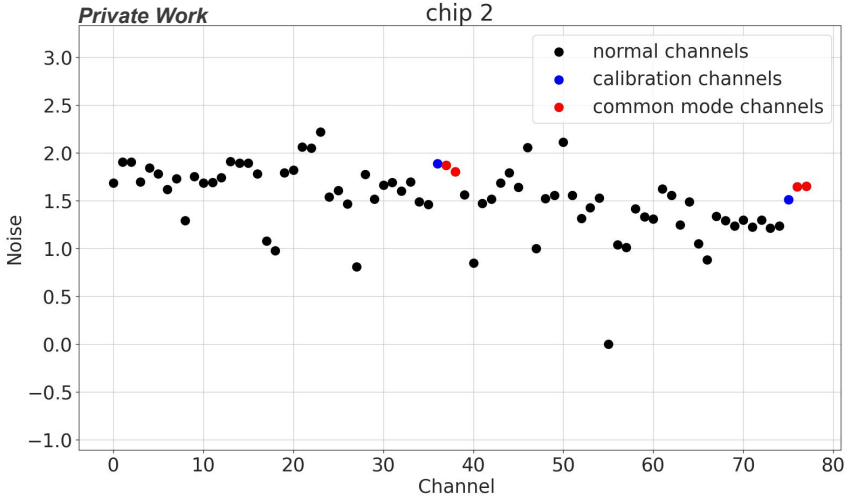
All 16 channels detected successfully

Tests after chip rework : pedestal run

- None of the channels in the above list shows noise to be zero (or some high value).
- Zero noise channels are the stuck channels (as discussed in the previous slides)
- In the current QC procedure, only pedestal and pedestal trimming is performed: would not pick up the unconnected channels

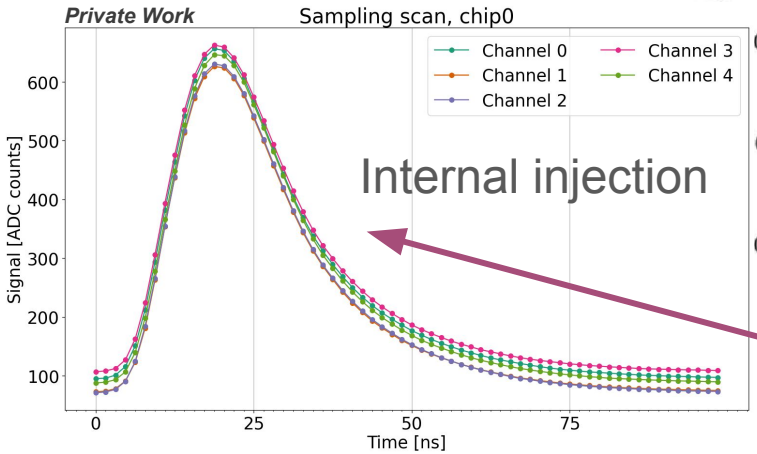




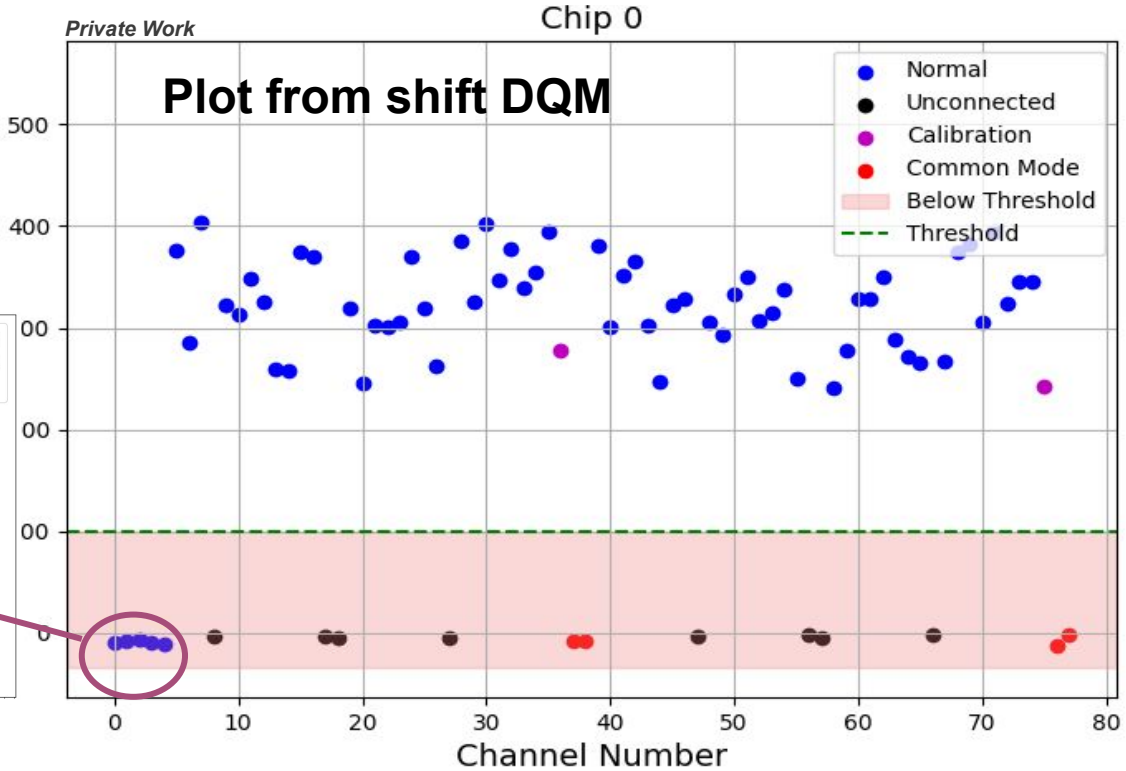


0 ADC response channels for board 412

Suspected disconnected channels
The internal injection for all these channels is working fine



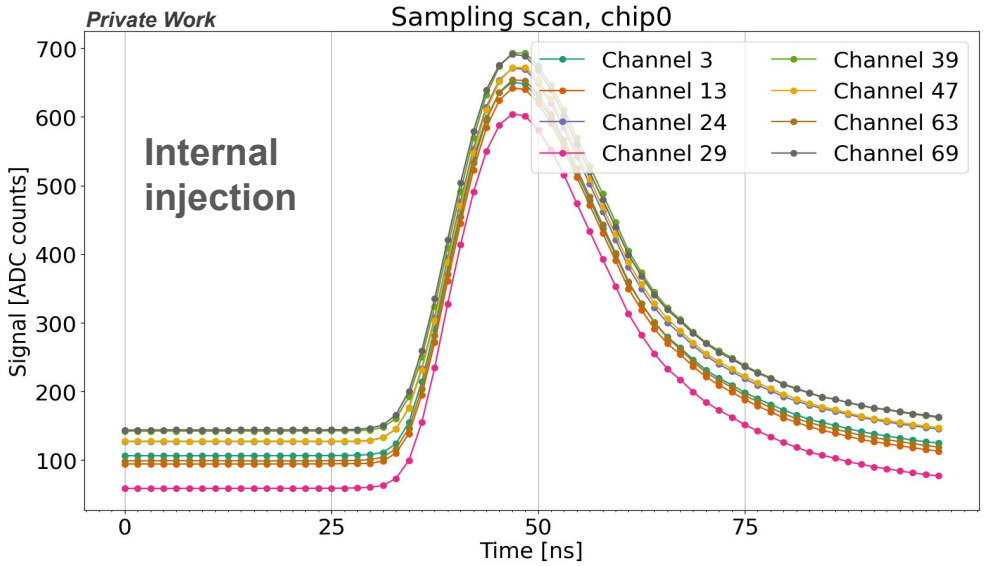
Internal injection



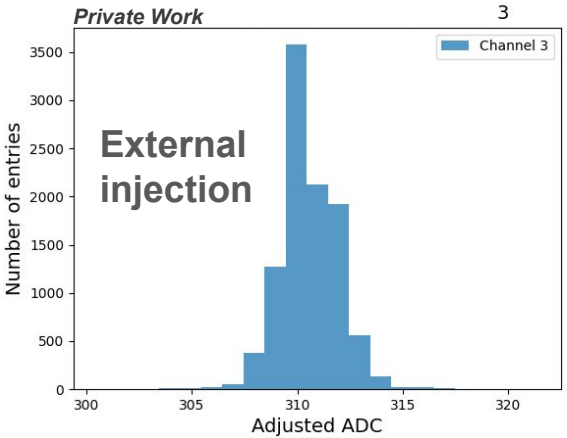
Checked the data with pressing the board but these channels still show ~ 0 ADC response. Checked this with five other similar boards, with pressing : still no difference from ~0 response in these channels.

Internal injection and external injection 1D distributions chip 0

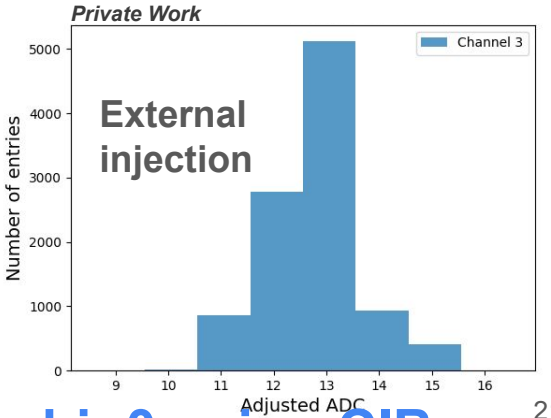
- List of channels made bad:
  1. Chip 0: 3, 13, 24, 29, 42(39), 50(47), 67(63), 72(69)
  2. Chip 1: 81(3), 91(13), 102(25), 107(29), 120(39), 128(47), 145(63), 150(69)
- **Successful in seeing internal injection for all of them, so nothing is bad with the chip**
- **These channels do not respond to external injection as expected**



Pedestal subtracted ADC distribution before chip rework



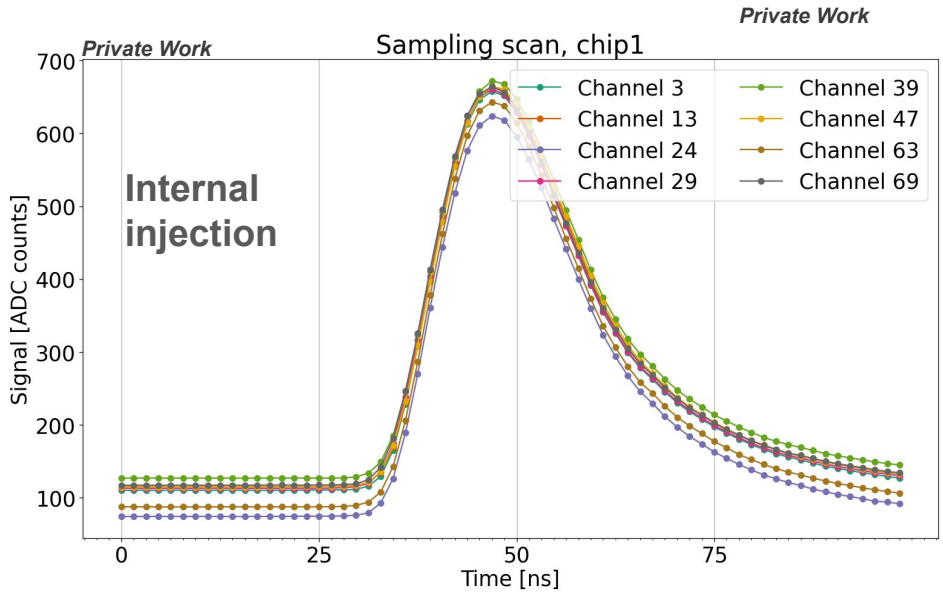
Pedestal subtracted ADC distribution after chip rework



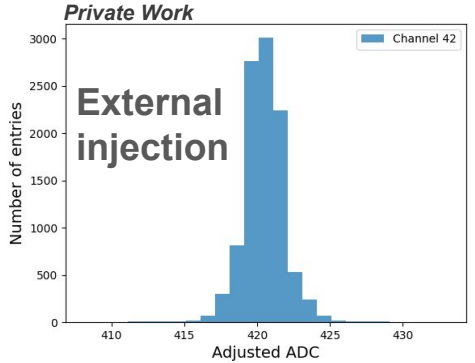
Successful detection of all the 8 bad channels in chip0 using CIB

Internal injection and external injection 1D distributions chip 1

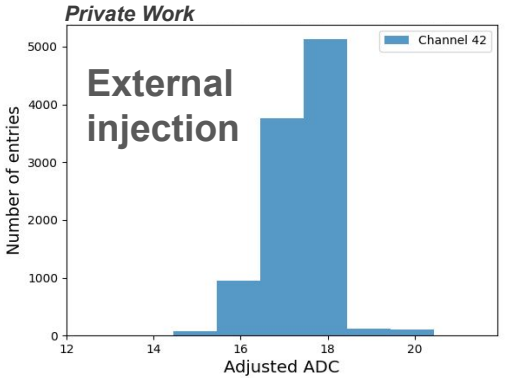
- List of channels made bad:
  1. Chip 0: 3, 13, 24, 29, 42(39), 50(47), 67(63), 72(69)
  2. Chip 1: 81(3), 91(13), 102(25), 107(29), 120(39), 128(47), 145(63), 150(69)
- **Successful in seeing internal injection for all of them**
- **These channels do not respond to external injection as expected**



Pedestal subtracted ADC distribution before chip rework

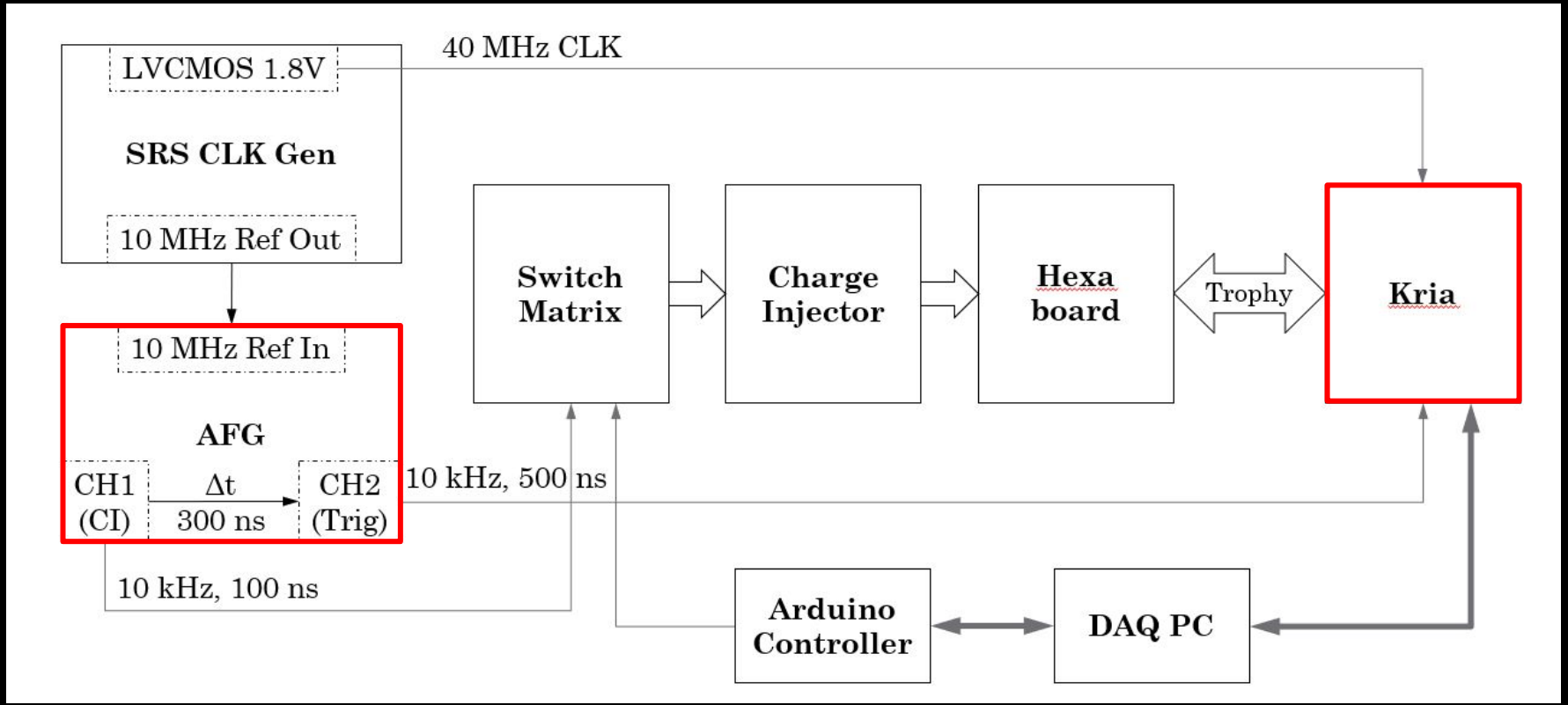


Pedestal subtracted ADC distribution after chip rework



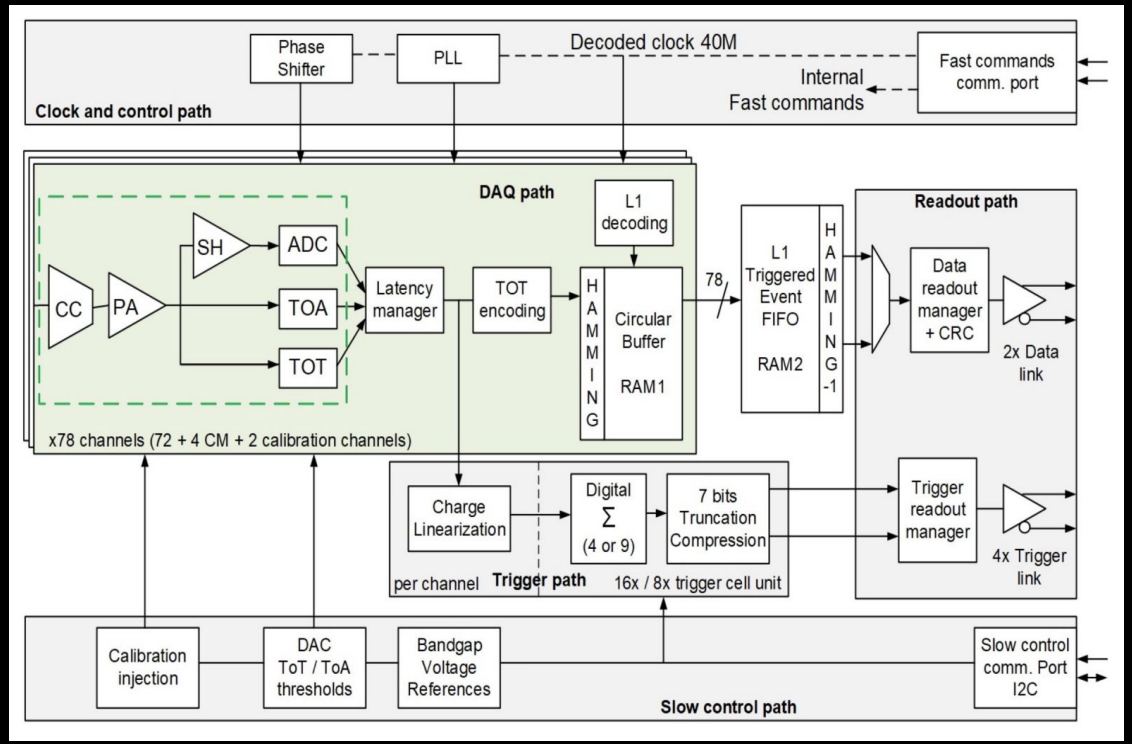
Successful detection of all the 8 bad channels in chip 1 using CIB

Why synchronous?

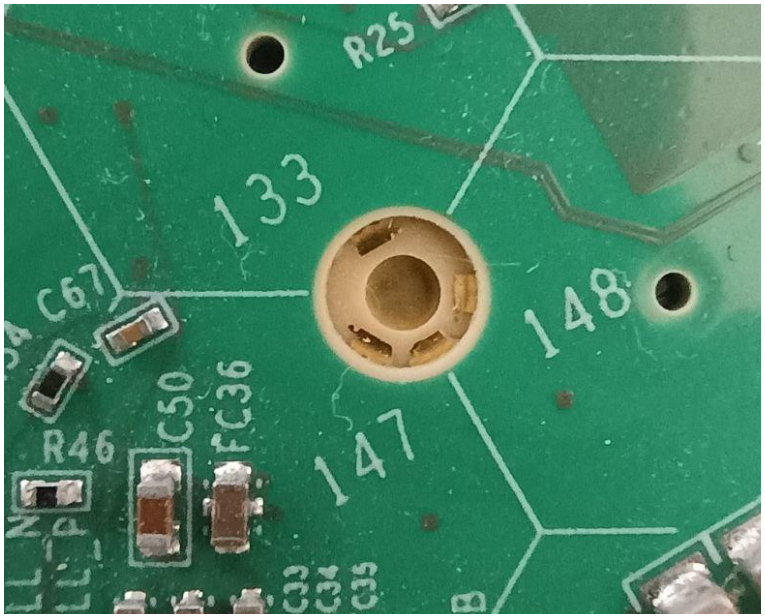


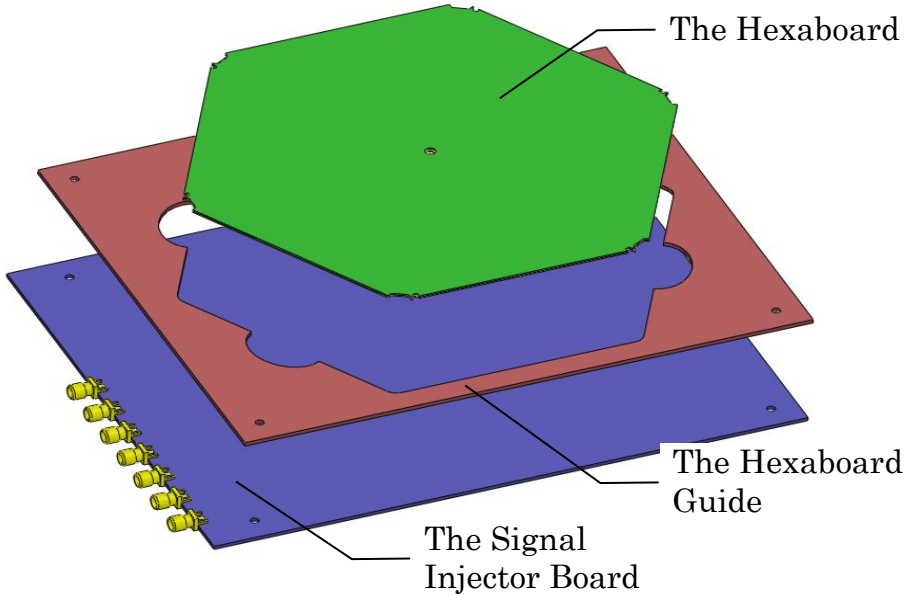
HGCROC chip

(1) One HGCROC has total 78 channels and a chip is divided into 2 halves:
>> 36 normal channels (4 unconnected from Si sensor)
>> 2 common mode channels
>> 1 calibration channels
(2) Internal injection

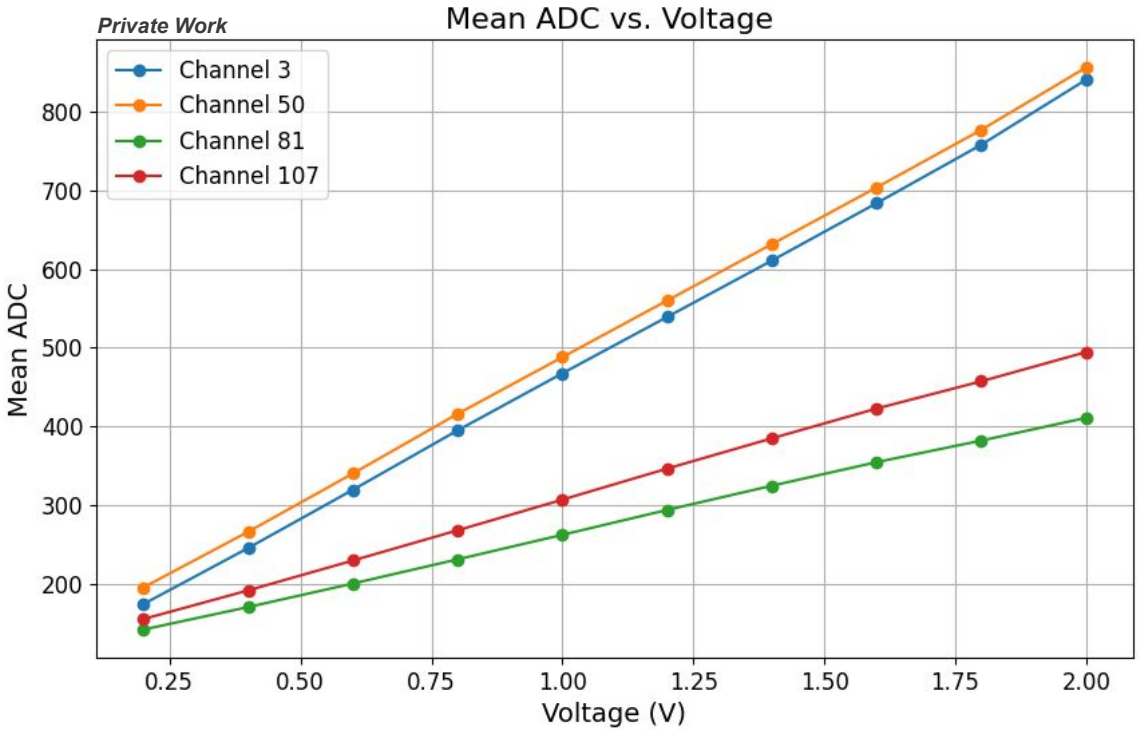


Placementof hexaboard on the charge injection board

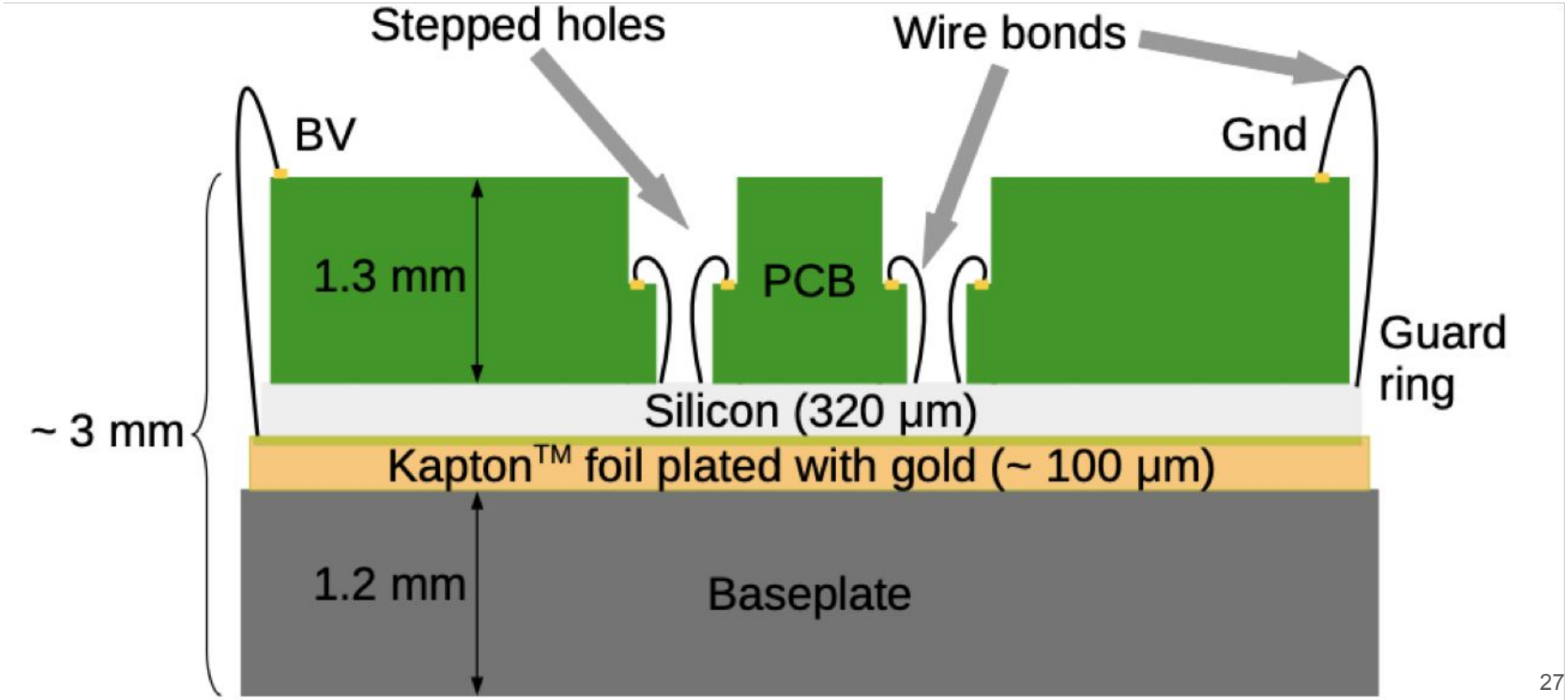




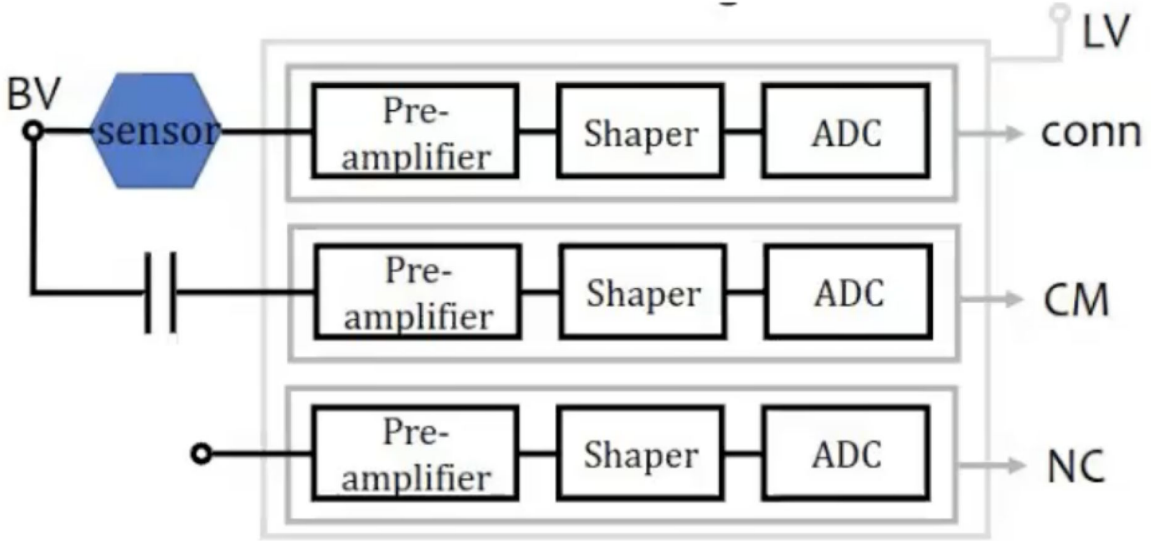
Before rework linearity



Hexamodule cross sectional view

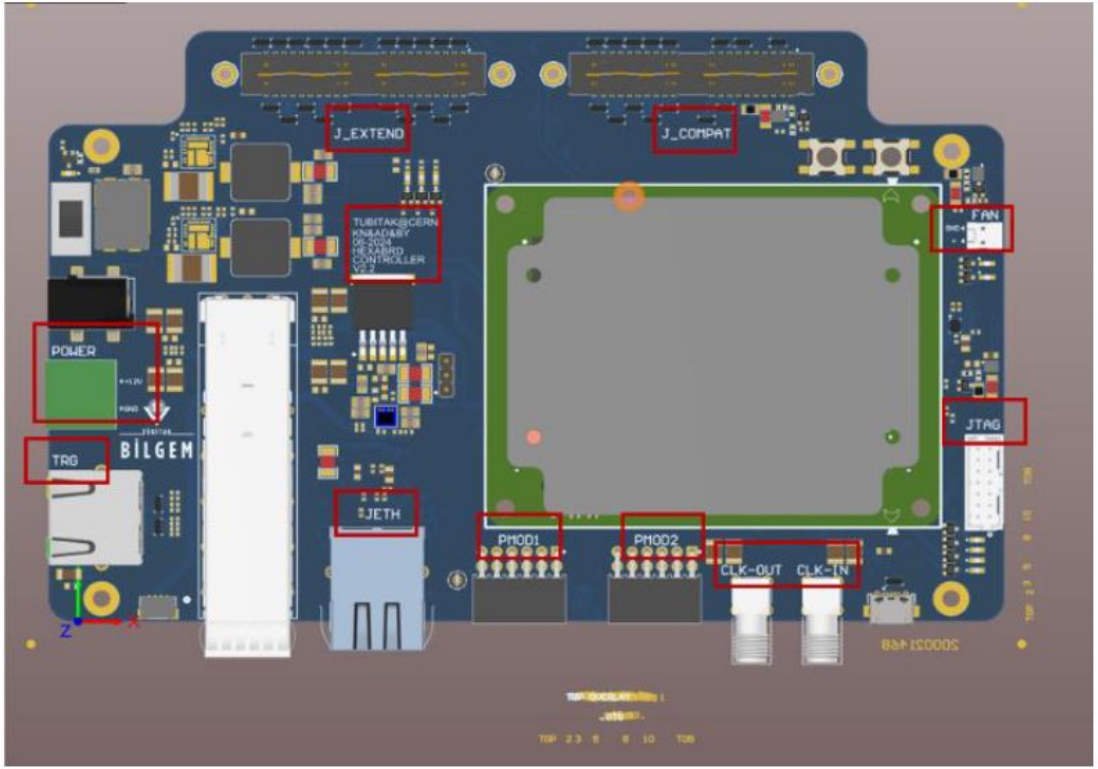


Chip basic structure and Hexaboard 8 layers

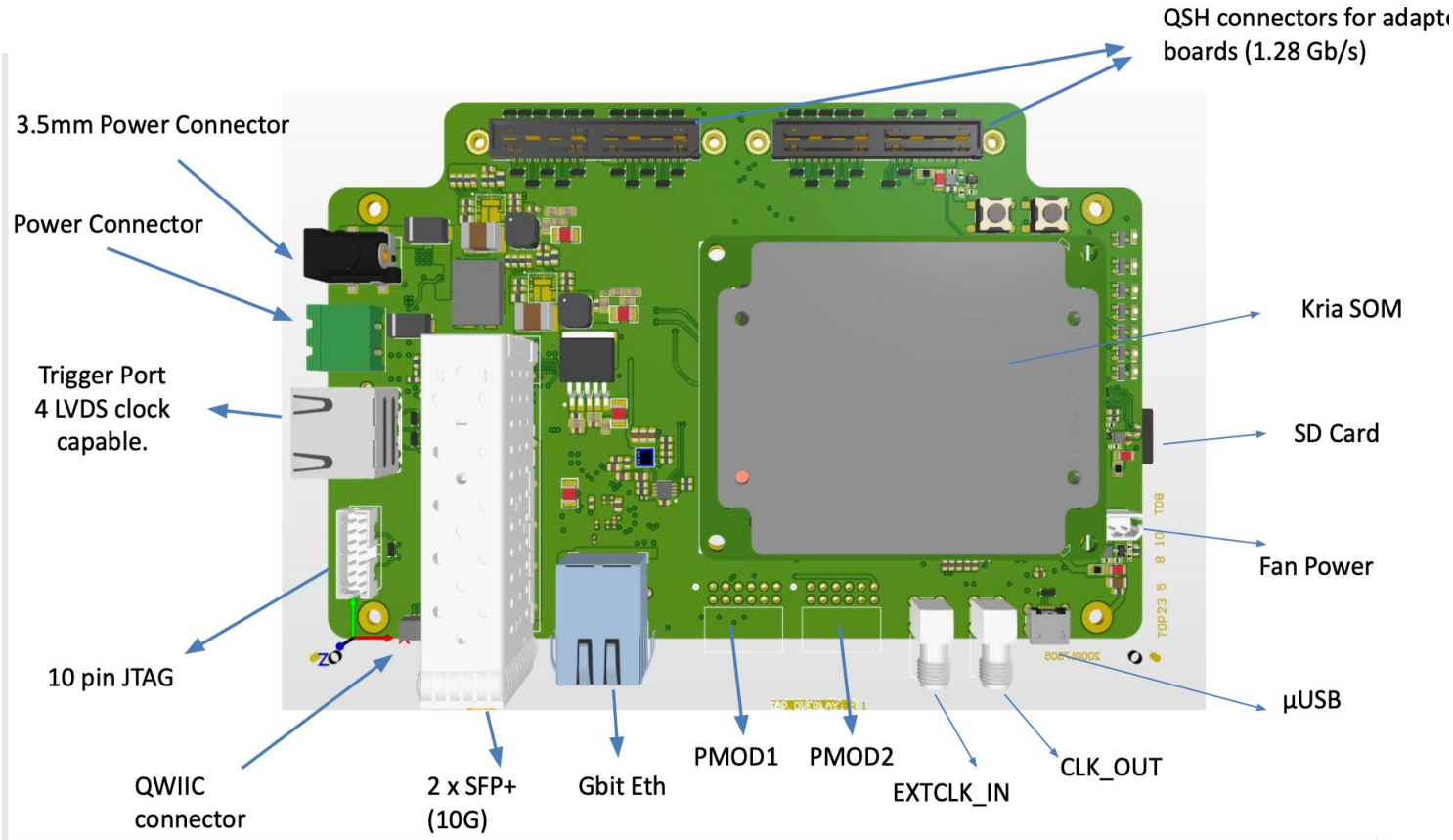


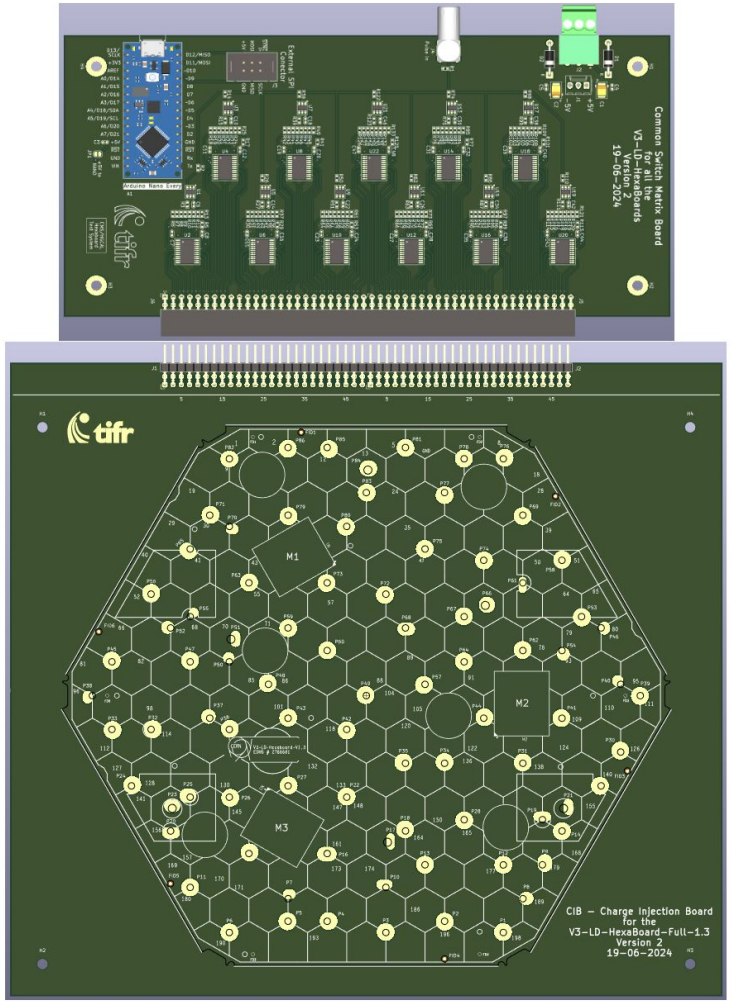
L1 320 M
FR4
L2. 1.28G
FR4
L3. **GND**
FR4
L4.**VDDA & VDDD**
FR4
L5. **GND**
FR4(No-flow Glue)
L6. **An. inputs**
FR4
L7. **GND**
FR4
L8.Empty

Kria


J_EXTEND
J_COMPAT
FAN
POWER
TRG
BİLGEM
JTAG
JETH
PMOD1
PMOD2
CLK-OUT
CLK-IN

Kria design


QSH connectors for adapt
boards (1.28 Gb/s)
3.5mm Power Connector
Power Connector
Trigger Port
4 LVDS clock
capable.
10 pin JTAG
QWIIC
connector
2 x SFP+
(10G)
Gbit Eth
PMOD1
PMOD2
EXTCLK_IN
CLK_OUT
µUSB
Fan Power
SD Card
Kria SOM


Common Switch Matrix Board
for the
V3-LD-HexaBoards
Version 2
19-06-2024
tifr
M1
M2
M3
CIB – Charge Injection Board
for the
V3-LD-HexaBoard-Full-1.3
Version 2
19-06-2024