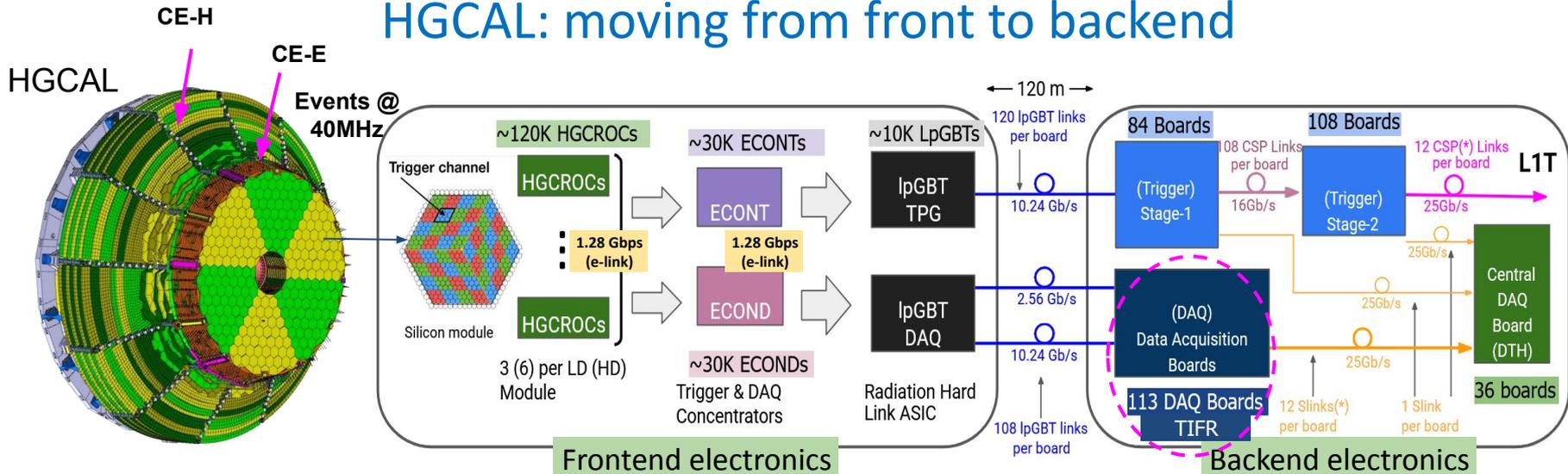


Overview of Development of CMS HGCAL Backend Electronics

DHEP Annual Meeting
March 16-17, 2026

Irfan Mirza, Chetan Mandloi, Gagan Mohanty
Department of High Energy Physics, TIFR
(In collaboration with the IISc-CMS group)

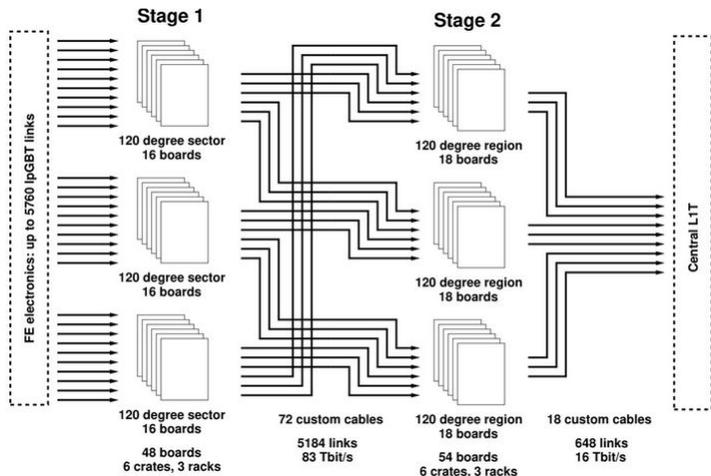
HGCAL: moving from front to backend



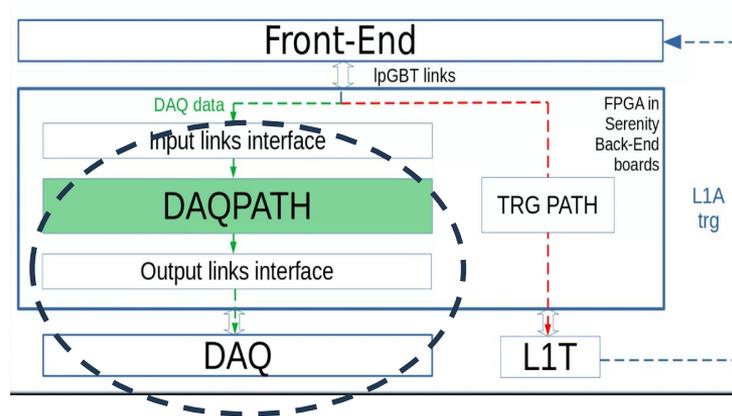
- **Electromagnetic section (CE-E):** 26 layers of hexagonal silicon sensors, comprising 100–400 hexagonal pad cells
- **Hadronic section (CE-H):** 21 layers of mixture of silicon sensors (near the beam pipe) and scintillator tiles (towards the periphery)
- Triggered event data are readout through **~6.3 million (silicon + scintillator)** readout channels with custom radiation-hard HGCROC ASICs generating digitized data, TOA, TOT
- **ECON-T (trigger path):** Concentrates trigger channel data via specific trigger algorithms (40 MHz)
- **ECON-D (DAQ path):** Channel alignment and zero suppression after Level-1 (L1) Accept and sends to DAQ (750 KHz)
- **IpGBT + VTRX (low Power Gigabit Transceiver + Optical Transceiver):** IpGBT, together with the VTRX+, serializes data and converts electrical signal to optical signal via 120 meter long fiber cables

Backend trigger and DAQ paths

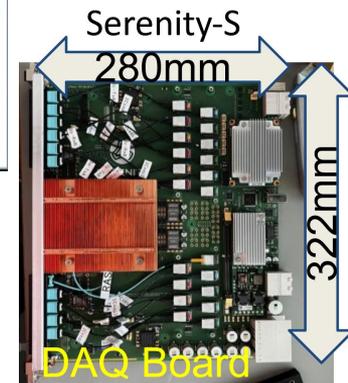
TPG System



- Generic ATCA (*Advanced Telecommunication Computing Architecture*) form factor for backend “**Serenity-S**” boards, common to other subsystems
- Stage 1: Receives the raw data from the frontend, selects trigger cells and adds individual module sums to partially form tower energies
- Stage 2: Performs trigger cell clustering (3D cluster objects) and calculates their positions, energies, and shape
- Coarse data @ 40MHz: ~70 Tb/s



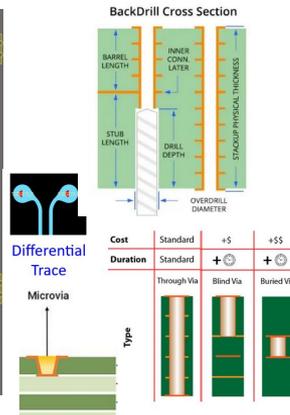
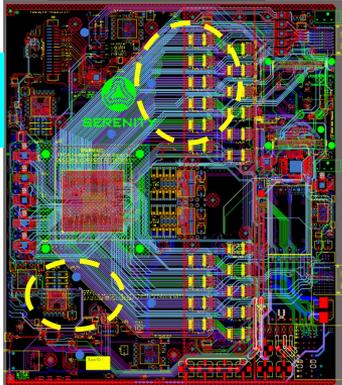
- Receives DAQ data from the FE links, buffers, decodes and forwards fully built events (fine-detailed) for every L1-trigger accept (750 KHz average rate)
- Distributes the slow control (configuration) and fast control (Clock and L1A distribution) to the front-end
- Fine Data @ 750 KHz: ~40Tb/s
- TIFR will deliver 113 DAQ boards (fabrication, assembly, and validation) as a part of Core Deliverables to CMS for HGCal



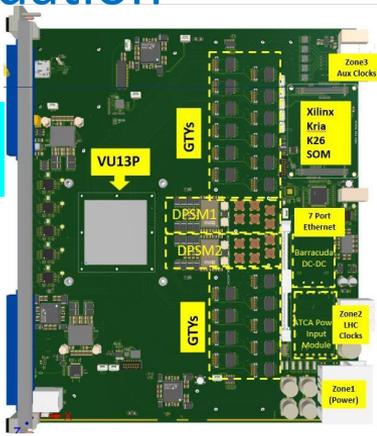
DAQ Serenity-S board design, development and validation

Layer	Stack up	Description	Process/Thickness
1	SEPI10V-01-1100M1-11111111	Tape PFR 4000 SP13M GREEN	1.000
2		Copper Pad 081224 T24 Holes-04P2-03P8-FIVEV	1.800
3		TU-ABSA SP 1035 RC58	0.304
4		TU-ABSA SP 3.0M1_HH11078x1	0.800
5		TU-ABSA SP 1035 RC58	0.304
6		TU-ABSA SP 1035 RC58	0.304
7		TU-ABSA SP 3.0M1_HH11078x1	0.800
8		TU-ABSA SP 1035 RC58	0.304
9		TU-ABSA SP 1035 RC58	0.304
10		TU-ABSA SP 3.0M1_HH11078x1	0.800
11		TU-ABSA SP 1035 RC58	0.304
12		TU-ABSA SP 1035 RC58	0.304
13		TU-ABSA SP 3.0M1_HH11078x1	0.800
14		TU-ABSA SP 1035 RC58	0.304
15		TU-ABSA SP 1035 RC58	0.304
16		TU-ABSA SP 3.0M1_HH11078x1	0.800
17		TU-ABSA SP 1035 RC58	0.304
18		Tape PFR 4000 SP13M GREEN	1.000

Design Layout

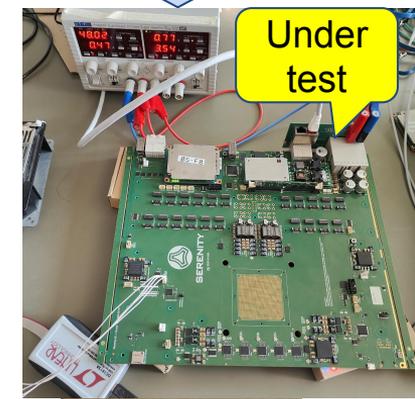
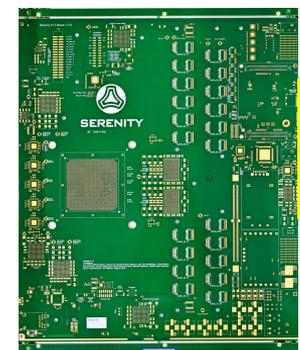
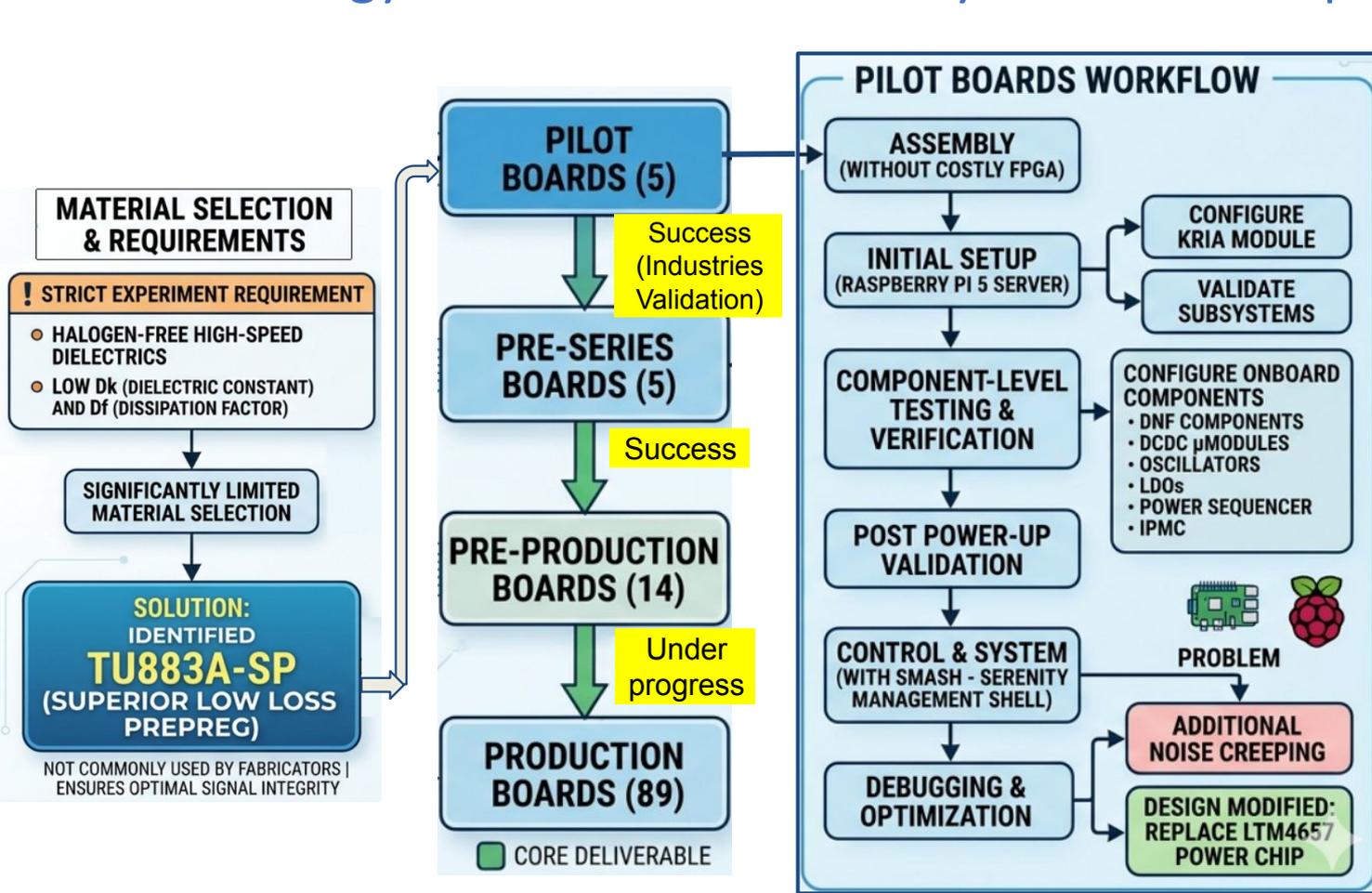


3D Rendering

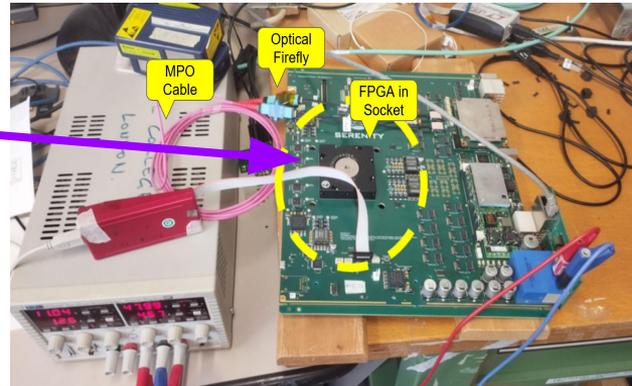
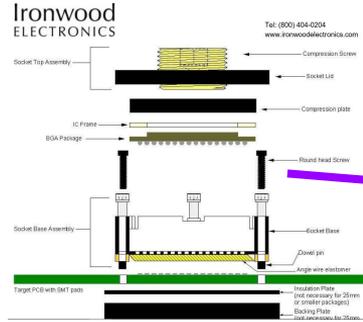
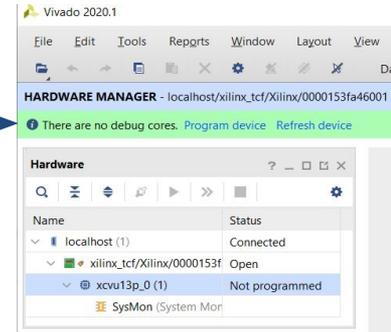


- Serenity-S, high-performance and production-ready platform built on the Serenity-Z prototyping to meet the enormous data volumes and challenging trigger requirements
- Features a production-grade Xilinx Virtex Ultrascale+ flipchip BGA FPGA (XCVU13P, 2577 pins, 52mm x 52mm x 4.5mm) and a Zynq Kria System-on-Module K26 (SoM, FPGA+Linux OS)
- Intricate 18 layers of HDI design layout is a teamwork of a team including TIFR (Backward Comp. XCVU9P FPGA), Imperial, and Karlsruhe
- Highly complex design (μ vias, blind vias, backdrilling) and hence technologically challenging to fabricate
- Developed symmetric stackup in consultation with fabricator for the design
- Bidirectional high-speed Multi-Gigabit Transceivers (MGTs): 120 (72N, 48S) (Data Rate: 28 Gbps per link)
- Intelligent Programmable Management Controller (IPMC) for housekeeping monitoring and control

Chronology and workflow: Serenity-S DAQ development @ TIFR



Pre-Series Board Performance Test

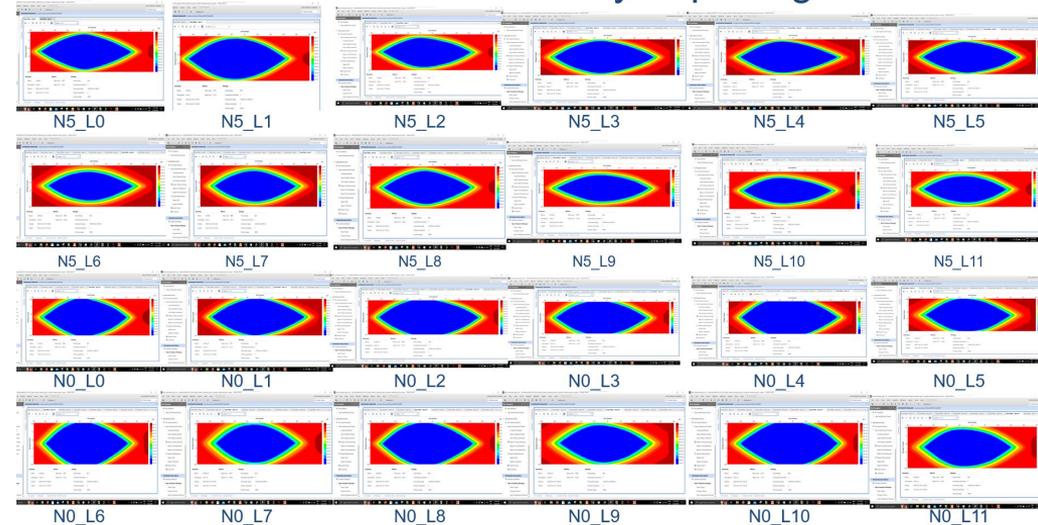
Copper
LoopbackSuccessful Interposer Socket
Assembly with VU13POptical
Firefly

- Pre-Series boards:
 - Three boards were assembled
 - One without FPGA
 - One with Dummy BGA (thermal profile verification during Reflow assembly)
 - One with real FPGA (XCVU13P-1 device) (full performance checks)
- Successful component-level functionality for all three boards except FPGA board
- Debugging, various checks suggested of poor FPGA assembly
- Disassembled the FPGA, interposer socket Assembly with FPGA on the same board to verify board performance
- Full functional tests with IBERT firmware for high-speed serial links (MGTs) performance with both copper loopback and firefly optics @ 25G including overnight performance runs
- Performances were satisfactory

Optical performance (N5-N0) for overnight run (for ~17 hrs)

Serial I/O Links							
Name	TX	RX	Status	Bits	Errors	TX Pol...	BER
Ungrouped Links (0)							
Link Group N5 (12)							
Link 0	Quad_221/MGT_X1Y7/TX (xcvu13p_0)	Quad_221/MGT_X1Y7/RX (xcvu13p_0)	25.594 Gbps	1.57E15	0E0		6.371E-16
Link 1	Quad_221/MGT_X1Y4/TX (xcvu13p_0)	Quad_221/MGT_X1Y4/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.371E-16
Link 10	Quad_223/MGT_X1Y12/TX (xcvu13p_0)	Quad_223/MGT_X1Y12/RX (xcvu13p_0)	25.598 Gbps	1.57E15	0E0		6.371E-16
Link 11	Quad_223/MGT_X1Y15/TX (xcvu13p_0)	Quad_223/MGT_X1Y15/RX (xcvu13p_0)	25.595 Gbps	1.57E15	0E0		6.371E-16
Link 2	Quad_222/MGT_X1Y8/TX (xcvu13p_0)	Quad_222/MGT_X1Y8/RX (xcvu13p_0)	25.604 Gbps	1.57E15	0E0		6.371E-16
Link 3	Quad_221/MGT_X1Y5/TX (xcvu13p_0)	Quad_221/MGT_X1Y5/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.371E-16
Link 4	Quad_222/MGT_X1Y9/TX (xcvu13p_0)	Quad_222/MGT_X1Y9/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.371E-16
Link 5	Quad_221/MGT_X1Y6/TX (xcvu13p_0)	Quad_221/MGT_X1Y6/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.371E-16
Link 6	Quad_222/MGT_X1Y10/TX (xcvu13p_0)	Quad_222/MGT_X1Y10/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.371E-16
Link 7	Quad_223/MGT_X1Y13/TX (xcvu13p_0)	Quad_223/MGT_X1Y13/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.371E-16
Link 8	Quad_222/MGT_X1Y11/TX (xcvu13p_0)	Quad_222/MGT_X1Y11/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.371E-16
Link 9	Quad_223/MGT_X1Y14/TX (xcvu13p_0)	Quad_223/MGT_X1Y14/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.371E-16
Link Group N0 (12)							
Link 0	Quad_121/MGT_X0Y7/TX (xcvu13p_0)	Quad_121/MGT_X0Y7/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.37E-16
Link 1	Quad_121/MGT_X0Y4/TX (xcvu13p_0)	Quad_121/MGT_X0Y4/RX (xcvu13p_0)	25.606 Gbps	1.57E15	0E0		6.37E-16
Link 10	Quad_123/MGT_X0Y12/TX (xcvu13p_0)	Quad_123/MGT_X0Y12/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.37E-16
Link 11	Quad_123/MGT_X0Y15/TX (xcvu13p_0)	Quad_123/MGT_X0Y15/RX (xcvu13p_0)	25.604 Gbps	1.57E15	0E0		6.37E-16
Link 2	Quad_122/MGT_X0Y8/TX (xcvu13p_0)	Quad_122/MGT_X0Y8/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.37E-16
Link 3	Quad_121/MGT_X0Y5/TX (xcvu13p_0)	Quad_121/MGT_X0Y5/RX (xcvu13p_0)	25.606 Gbps	1.57E15	0E0		6.37E-16
Link 4	Quad_122/MGT_X0Y9/TX (xcvu13p_0)	Quad_122/MGT_X0Y9/RX (xcvu13p_0)	25.595 Gbps	1.57E15	0E0		6.37E-16
Link 5	Quad_121/MGT_X0Y6/TX (xcvu13p_0)	Quad_121/MGT_X0Y6/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.37E-16
Link 6	Quad_122/MGT_X0Y10/TX (xcvu13p_0)	Quad_122/MGT_X0Y10/RX (xcvu13p_0)	25.608 Gbps	1.57E15	0E0		6.37E-16
Link 7	Quad_123/MGT_X0Y13/TX (xcvu13p_0)	Quad_123/MGT_X0Y13/RX (xcvu13p_0)	25.606 Gbps	1.57E15	0E0		6.37E-16
Link 8	Quad_122/MGT_X0Y11/TX (xcvu13p_0)	Quad_122/MGT_X0Y11/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.37E-16
Link 9	Quad_123/MGT_X0Y14/TX (xcvu13p_0)	Quad_123/MGT_X0Y14/RX (xcvu13p_0)	25.600 Gbps	1.57E15	0E0		6.37E-16

Eye-Diagrams with Fireflies (N5-N0) Eye openings : 60-75%



Total 10 Quads

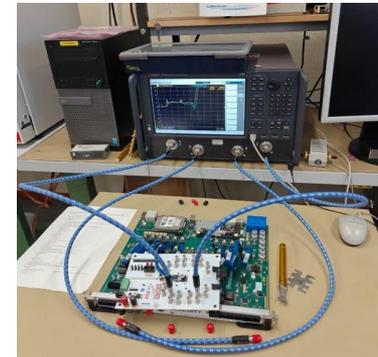
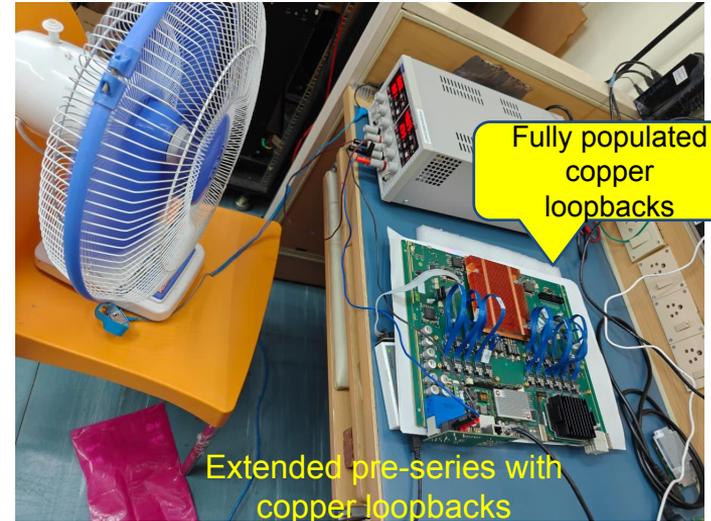
Each Quad carries 12 links

North Section: 6 Quads, South Section: 4 Quads

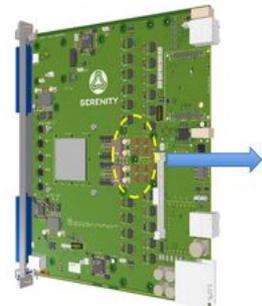
Similar link evaluation run for all North (N1-N2, N3-N4) and South Fireflies (S0-S1, S2-S3) were found error-free

Extended pre-series board performance test

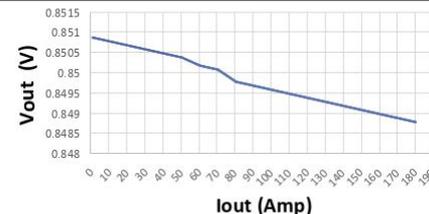
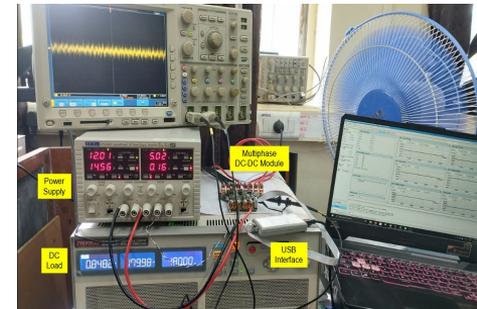
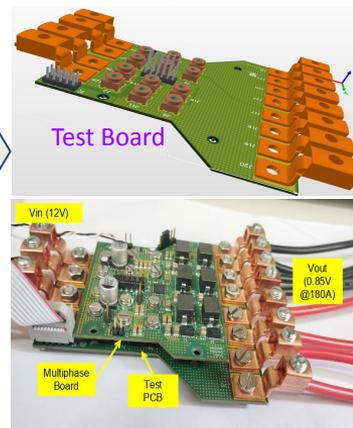
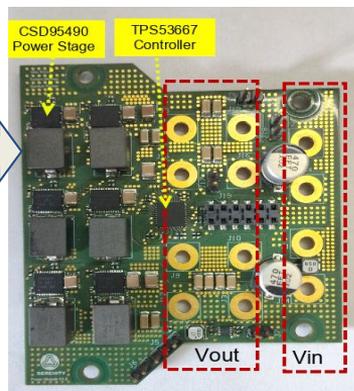
- Extended preseries boards:
 - Two boards fully assembled with FPGA (XCVU13P-2) devices
 - High power performance test with fully populated copper loopback and firefly optics tests were performed
 - Eye diagrams showed an excellent 60-75% eye opening, which is a testament to the high quality of the PCB manufacturing and assembly
 - Extended overnight tests were carried out with fully populated copper loopbacks validating fabrication-assembly capabilities of Indian Industries
- Results:
 - A few high speed links in one of the boards with some random errors observed during overnight run and functional validation.
 - Debug tests with Time Domain Reflectometer (TDR) for error generating high speed links were done to provide feedback to the fabricator
- Pre-production boards: We now developing 14 pre-production boards to be supplied to CERN as a part of core deliverables



Design, development, and validation of multiphase DC-DC converter



Parameter	Value	Description
Vin	7- 17V (DC)	Backplane Power Source
Vout (VccInt)	0.85V (DC)	FPGA Core Voltage
Imax	180A	Operating @ ~150A
Vo(ripple)	5mV@180A	Tolerance for FPGA



- XCVU13P FPGA requires a substantial core current of up to 150A at 0.85V when fully operational provided by LTM4700 modules (DPSM)
- Availability of DPSM is volatile due to semiconductor industry fluctuations (40-50 weeks or more)
- In absence of DPSM, Serenity-S can work with the Mezzanine Power Module
- Fully in-house development (8-Layers) of Mezzanine Power Module (78mm x 67mm) at TIFR
- It is a 6 phase PMBUS controlled multiphase DC-DC Converter with PWM controller (TPS53667) and 6 power stages (CDS95490) with telemetry i.e.voltage, current, temperature, and fault status
- Converter was stress-tested with aggressive current ramps (120A, 180A) to ensure stability under dynamic load changes with electronic DC Load (ProDigit: 3352F)
- Ripple (max. ~5 mVp-p) measured on the output voltage at a 180 A load, Load Regulation better than 1%, Efficiency @ ~87%
- **Conclusion: Multiphase DC-DC converter meets all design specifications and provides a verified alternative to the LTM4700**

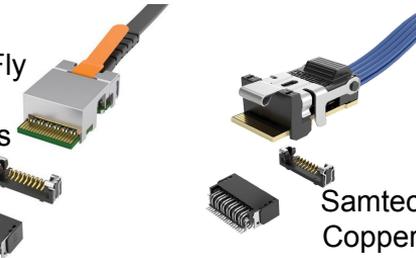
FAT and UAT testing of Serenity-S

- Infrastructure and test setup:
 - Functional performance testing of Serenity-S boards during pre-production and production run will be performed at IISc for Factory Acceptance Test (FAT) as well as at TIFR for User Acceptance Test (UAT)
 - Common testing infrastructure and instruments for TIFR and IISc in place
 - ATCA Crates (6U) and Shelf Manager ✓
 - Programmable DC power supply ✓
 - SAMTEC Copper loopback cables ✓
 - SAMTEC Firefly optics ✓
 - Short Detection H/W DAQ 9600 ✓
 - DAQ-9600 with 40 channel Multiplexer(DAQ-903) ✓
 - Debuggers (LTM, TI, Pi Pico) ✓
 - TIFR has made infrastructural setup at IISc, trained the FAT personnels and will manage their supervision
 - TIFR will repeat FAT as well as perform more tests, including optics and endurance tests under UAT

Programmable DC Power Supply



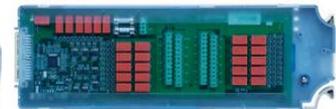
Samtec FireFly Optical Transceivers



Samtec Copper loopback



[DAQ-9600-GPIB](#)



[Multiplexer modules](#)

Summary

- Pilot boards (S1.1): fabrication, assembly, commissioning, and functional testing validated the development goals
- Pre-series boards (S1.2, S1.3): fabrication, assembly, commissioning and diligent board level functional testing
- Extended pre-series (S1.4.0) boards were shipped to CERN
- Plans to fabricate 14 (pre-production) are in place and will be fabricated with Serenity-S 1.4.2
- After that, we will then go for 89 production board fabrication and assembly

Thank You

Testing Plans for FAT and UAT

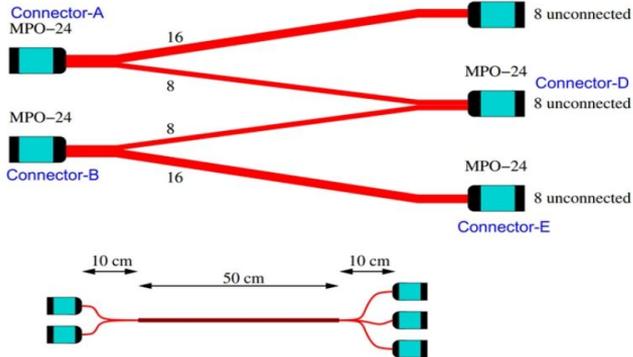
- FAT by the IISc will involve:
 - a. Visual Inspection
 - b. Short-circuit test
 - c. Sense Resistor check
 - d. Voltage and Board protection checks (OT, OV, UV etc.)
 - e. Functional checks with Kria, IPMC and M.2 for
 - i. Ethernet, I2Cs, LEDs, UART, JTAG,
 - ii. Transceivers and Clock tests
 - iii. Programming the FPGA
 - iv. Validation of High Speed MGT links via Copper loopback
- TIFR will guide IISc for some of the aforementioned testes as they are highly specialised
- UAT to be performed at TIFR includes:
 - a. Repetition of FAT
 - b. Validation of High Speed MGT links via Firefly optics and use PRBS to verify performance
 - c. High Power test with FPGA
 - d. Endurance tests with repeated configuration and long runtime tests
 - e. Some DAQ-specific tests unique to TIFR-UAT (will be more thorough compared to those performed at CERN to minimize logistical issues)

DAQ to DTH Board Cable (Test Sample)

Diagram + Pin Mapping:

Source: Gregory Iles

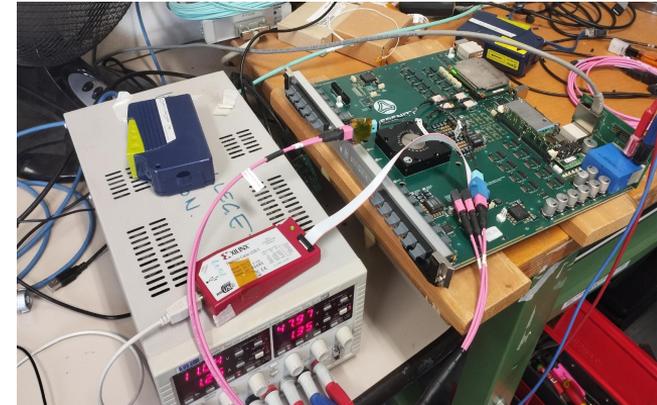
DAQ to DTH cable: 48 needed



Connection Table		Connection Table	
Input Female Connector Fiber	Output Female Connector Fiber	Input Female Connector Fiber	Output Female Connector Fiber
A1 (Rx 0)	C12 (Rx 0)	B1 (Rx 0)	E12 (Rx 0)
A2 (Rx 1)	C11 (Rx 1)	B2 (Rx 1)	E11 (Rx 1)
A3 (Rx 2)	C10 (Rx 2)	B3 (Rx 2)	E10 (Rx 2)
A4 (Rx 3)	C9 (Rx 3)	B4 (Rx 3)	E9 (Rx 3)
A5 (Rx 4)	C8 (Rx 4)	B5 (Rx 4)	E8 (Rx 4)
A6 (Rx 5)	C23 (Rx 5)	B6 (Rx 5)	E23 (Rx 5)
A7 (Rx 6)	C22 (Rx 6)	B7 (Rx 6)	E22 (Rx 6)
A8 (Rx 7)	C21 (Rx 7)	B8 (Rx 7)	E21 (Rx 7)
A9 (Rx 8)	D12 (Rx 0)	B9 (Rx 8)	D24 (Rx 4)
A10 (Rx 9)	D11 (Rx 1)	B10 (Rx 9)	D23 (Rx 5)
A11 (Rx 10)	D10 (Rx 2)	B11 (Rx 10)	D22 (Rx 6)
A12 (Rx 11)	D9 (Rx 3)	B12 (Rx 11)	D21 (Rx 7)
A13 (Tx 0)	C1 (Tx 0)	B13 (Tx 0)	E1 (Tx 0)
A14 (Tx 1)	C2 (Tx 1)	B14 (Tx 1)	E2 (Tx 1)
A15 (Tx 2)	C3 (Tx 2)	B15 (Tx 2)	E3 (Tx 2)
A16 (Tx 3)	C4 (Tx 3)	B16 (Tx 3)	E4 (Tx 3)
A17 (Tx 4)	C13 (Tx 4)	B17 (Tx 4)	E13 (Tx 4)
A18 (Tx 5)	C14 (Tx 5)	B18 (Tx 5)	E14 (Tx 5)
A19 (Tx 6)	C13 (Tx 6)	B19 (Tx 6)	E13 (Tx 6)
A20 (Tx 7)	C16 (Tx 7)	B20 (Tx 7)	E16 (Tx 7)
A21 (Tx 8)	D1 (Tx 0)	B21 (Tx 8)	D13 (Tx 4)
A22 (Tx 9)	D2 (Tx 1)	B22 (Tx 9)	D14 (Tx 5)
A23 (Tx 10)	D3 (Tx 2)	B23 (Tx 10)	D15 (Tx 6)
A24 (Tx 11)	D4 (Tx 3)	B24 (Tx 11)	D16 (Tx 7)

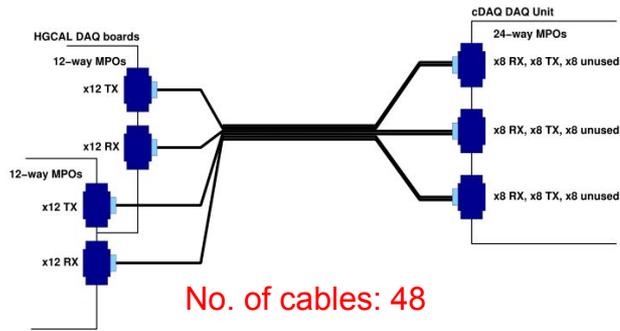


- Identified potential vendors for custom fiber-optic cables; most of them are ready to supply the cables with technical compliance reports, viz., insertion and return loss
- Worked out technical details with the above suppliers
- Made out few sample cables, test reports (I/L, R/L), microscopic QC
- One such cable provided to CMS for initial assessment
- Successful optical Integrity test was carried out with IBERT (CERN)

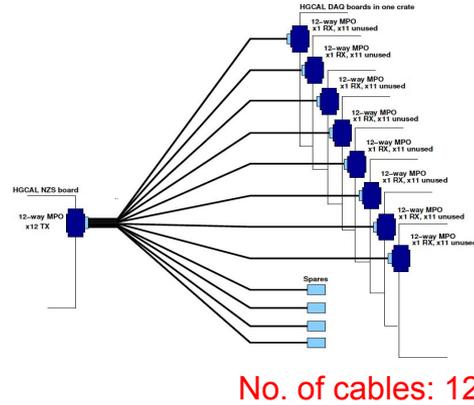


Optical Cable Deliverables

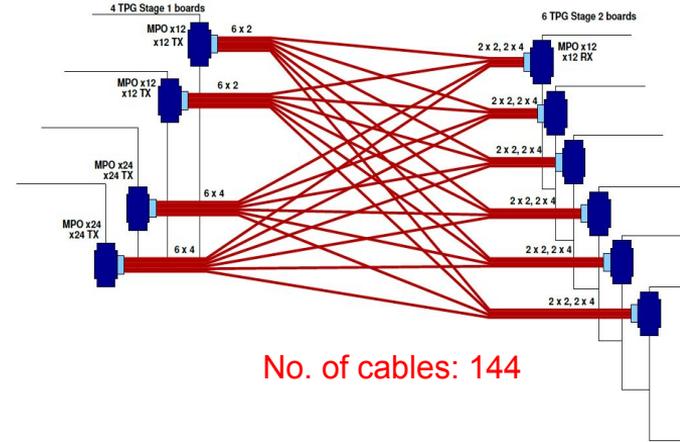
DAQ to DTH board cables (Updated)



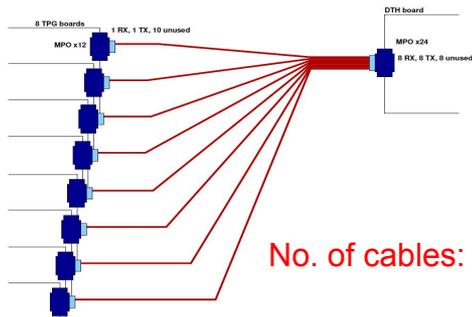
NZS board to DAQ board cables



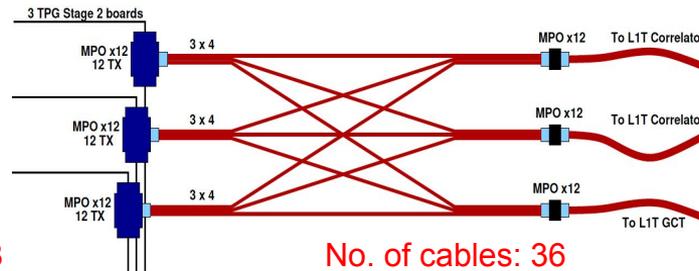
TPG Stage 1 to Stage 2 board cables



TPG Stage 1-2 to DTH board cables

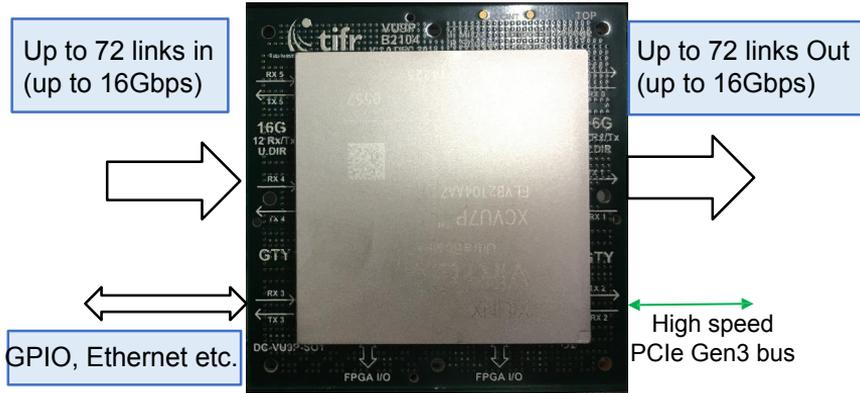


TPG Stage 2 to L1T board cables

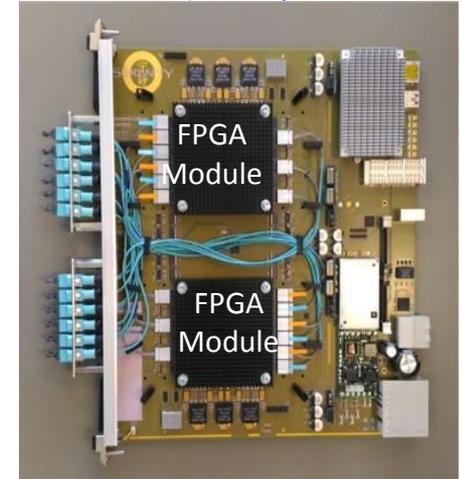


Development and Contribution @ TIFR: DC (Daughter Card)

ATCA Carrier card – Serenity Z1.0 designed at Imperial College
<http://serenity.web.cern.ch/>



Xilinx Virtex Ultrascale+ FPGA based plug-in module.
Designed and developed at TIFR



- Complete in-house design (16 layers, 64mm x 64mm) and indigenous manufacturing in India
- One of the high-performance FPGA (Xilinx VU7P/VU9P) based DC layout designed at TIFR
- Two variant DCs: SO1 (16G–16G), SM1 (16G–25G), Total throughput ~2 Tbps
- 72+72 high-speed serial links (25G) per lane (tested up to 16 Gbps) – Total throughput ~ 2 Tbps
- Fabrication (January 2020), Assembly (February 2020), and Testing (September 2020)
- Serenity Z1.1 fabricated by TIFR (1st Quarter of 2021)
- 280mm x 322mm, HDI design, Extensive μ vias (blind, buried), backdrillings, lengthy differential traces with narrow width/spacing (3mil/4mil)

