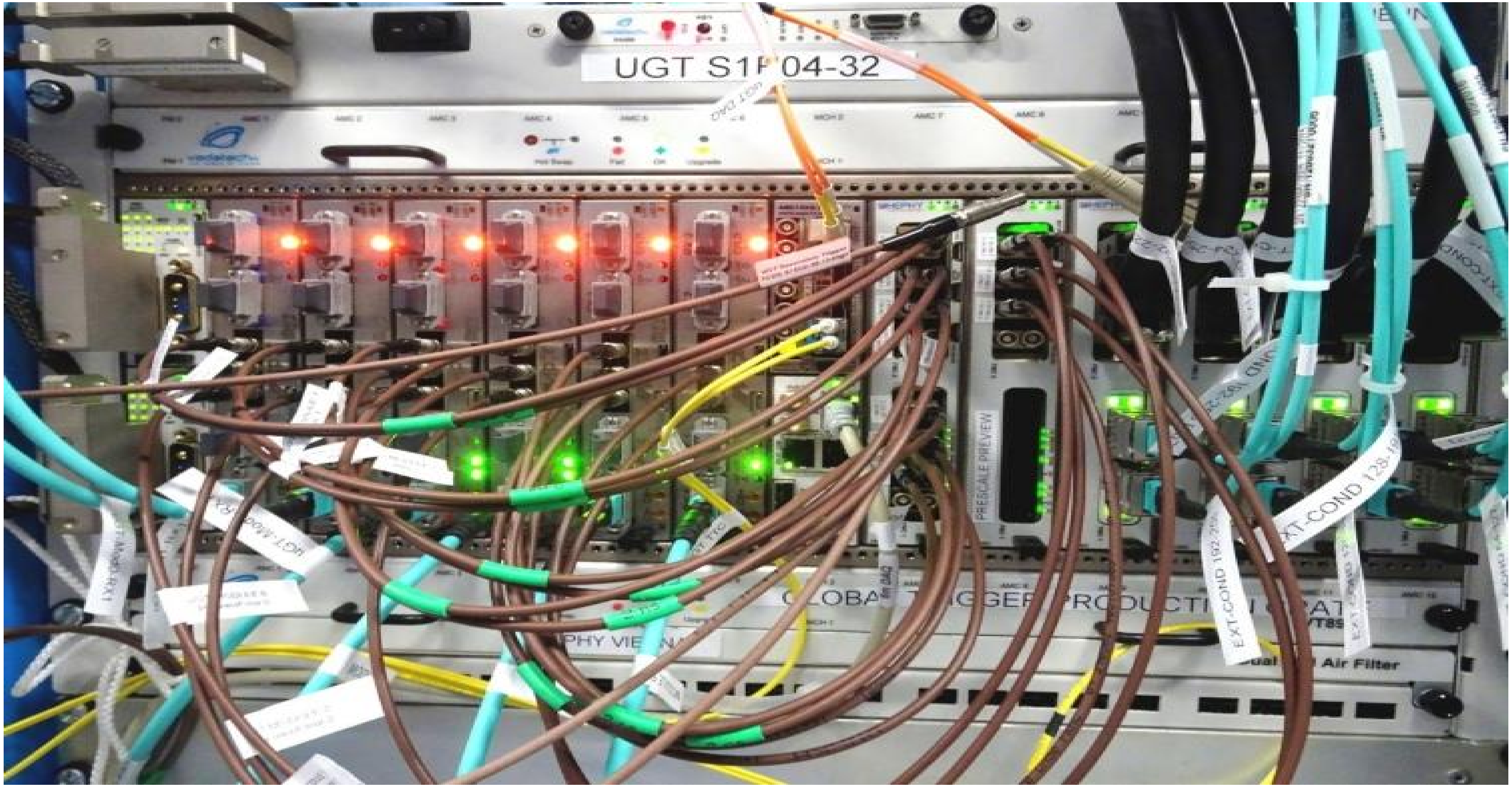
CMS L1 Trigger Upgrades for the HL -LHC



CMS L1 Trigger System

Trigger: Complex decision in few μs!

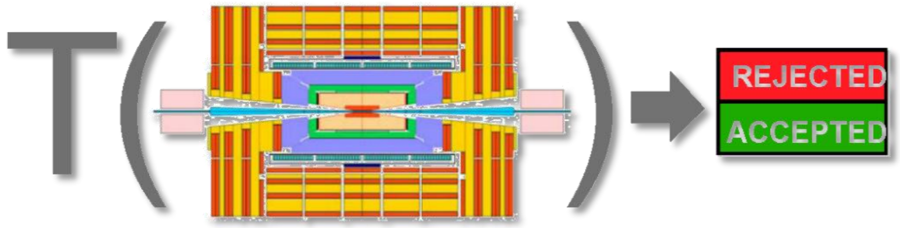
Level 1 Trigger (L1T)

- Receives detector data at the full 40MHz collision rate of LHC.
- Performs a fast reconstruction of each event.
- Determines whether the event should be read out from the detector.

---- Initially reconstructs particles within one sub-detector (regional)
----Finally combines all information for a global picture of the event before the trigger decision (global)

- **Task: inspect detector information and provide a first decision on whether to keep the event or throw it out**

The trigger is a function of :



Event data & Apparatus
Physics channels & Parameters

- **Detector data not (all) promptly available**
- **Selection function highly complex**

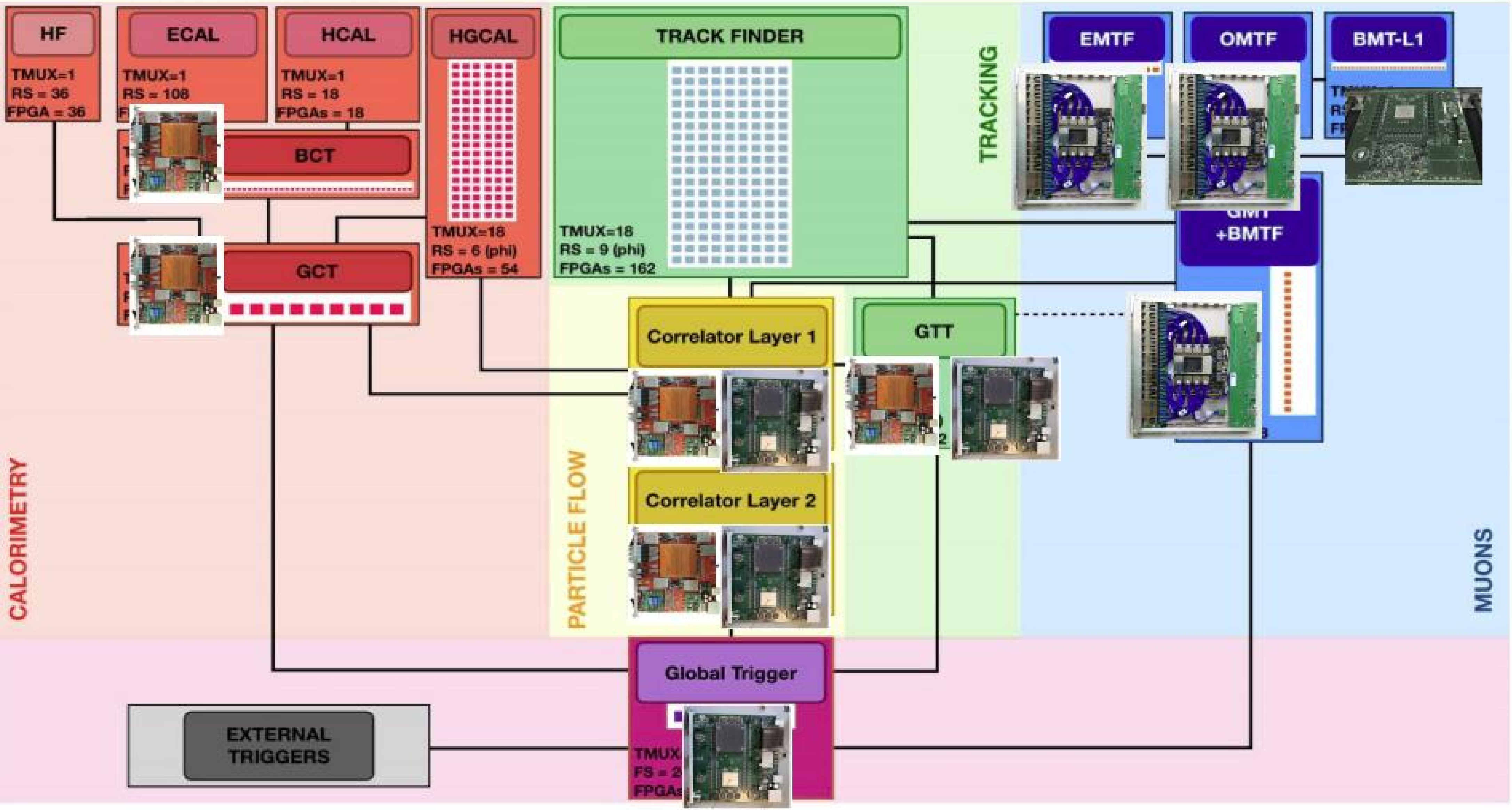
⇒T(...) is evaluated by successive approximations, the TRIGGER LEVELS
(possibly with zero dead time)

CMS L1 TRIGGER

- *Event rate increases with instantaneous luminosity (L)*
- Task of Trigger is to judiciously identify interesting events out of much larger number of mundane events, AND within an extremely short time so as not to loose the next event which may be interesting again!
- Note that occurrence of interesting event is completely random.
- Main challenges at high L (by 2028expect 5-7 * $10^{34}/cm^2/s$)
- a) large data throughput from the detector at a collision rate of 40 MHz
- b) 12 μs (presently 4 μs) latency to combine information from all subsystems
- **Dedicated all-FPGA hardware systems with time-multiplexed architecture**
- The first layer of the trigger requires a powerful, flexible and compact processing cards positioned at the backend of the detector readout system

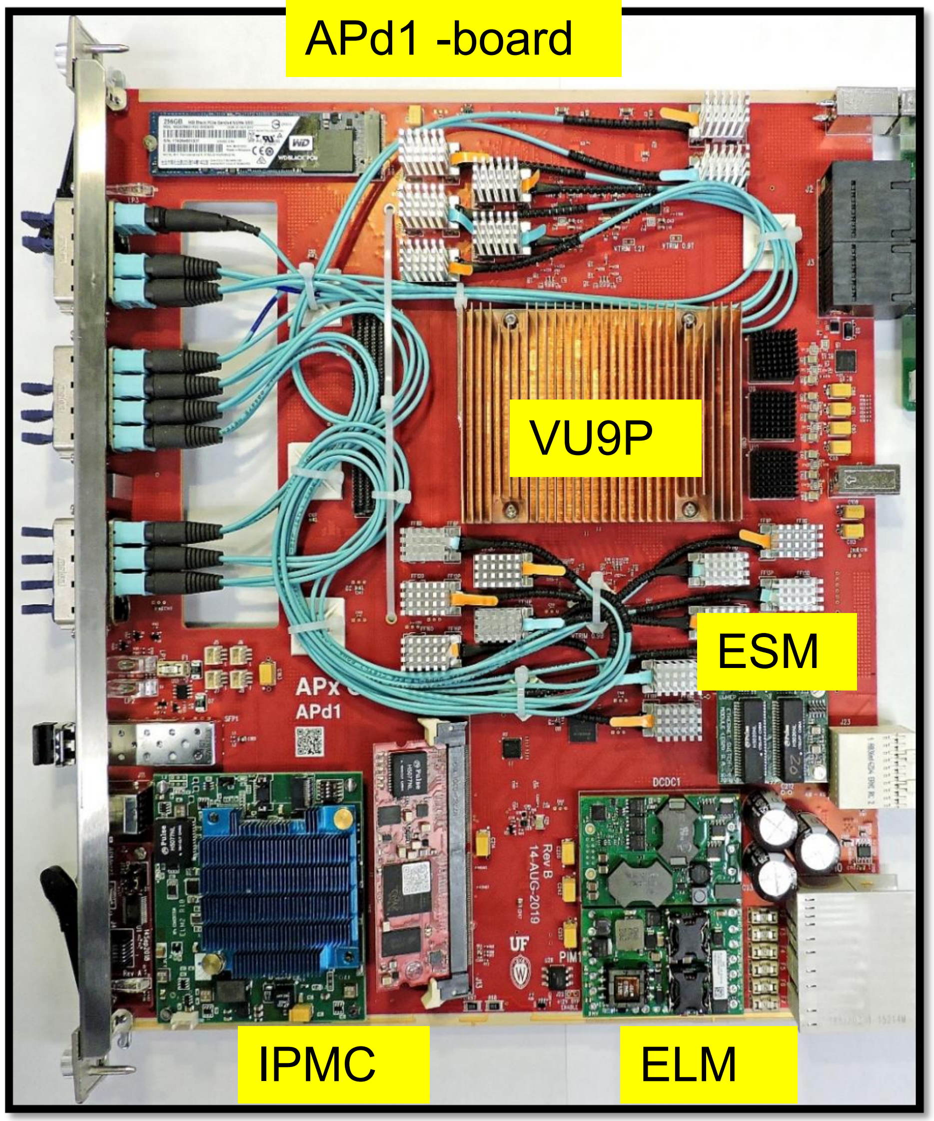
➔ custom-made hardware based on ATCA (Advanced Telecommunication Architecture)

Board map



HF
TMUX=1
RS = 36
FPGA = 36
ECAL
TMUX=1
RS = 108
HCAL
TMUX=1
RS = 18
FPGAs = 18
BCT
GCT
HGCAL
TMUX=18
RS = 6 (phi)
FPGAs = 54
TRACK FINDER
TMUX=18
RS = 9 (phi)
FPGAs = 162
TRACKING
EMTF
OMTF
BMT-L1
+BMTF
Correlator Layer 1
GTT
Correlator Layer 2
PARTICLE FLOW
CALORIMETRY
MUONS
Global Trigger
EXTERNAL TRIGGERS

Hardware efforts : Peripheral Boards for APd1



APd1 –Advanced Processor demo board-The Main calorimeter Trigger Board powered by a VU13P (Virtex 13 Ultrascale) FPGA with 2.5M logic cells and 100 bidirectional links upto 28Gbps

--- Three daughter boards that are mezzannine ot this Main board are ESM,IPMC and ELM (now Kria) board

ESM- Ethernet Switch Module

IPMC -Intelligent Platform Management controller

The above multilayer electronic boards were made in collaboration with Indian Industries (Micropack and Penisnula Electronics,and Electrowing @Bengaluru) and the quality control of all of them done in house labs

Mezzanine boards from TIFR

- **IPMC (Intelligent Platform Management Controller)**

--Negotiates with crate for power, connectivity

--Controls power, monitors board conditions via sensors

-Monitoring Hardware –System Temperature and Power Supply

--Provides lower level configuration support (Recovery Control) I,e Booting ,Restarting and Shutting down the Server

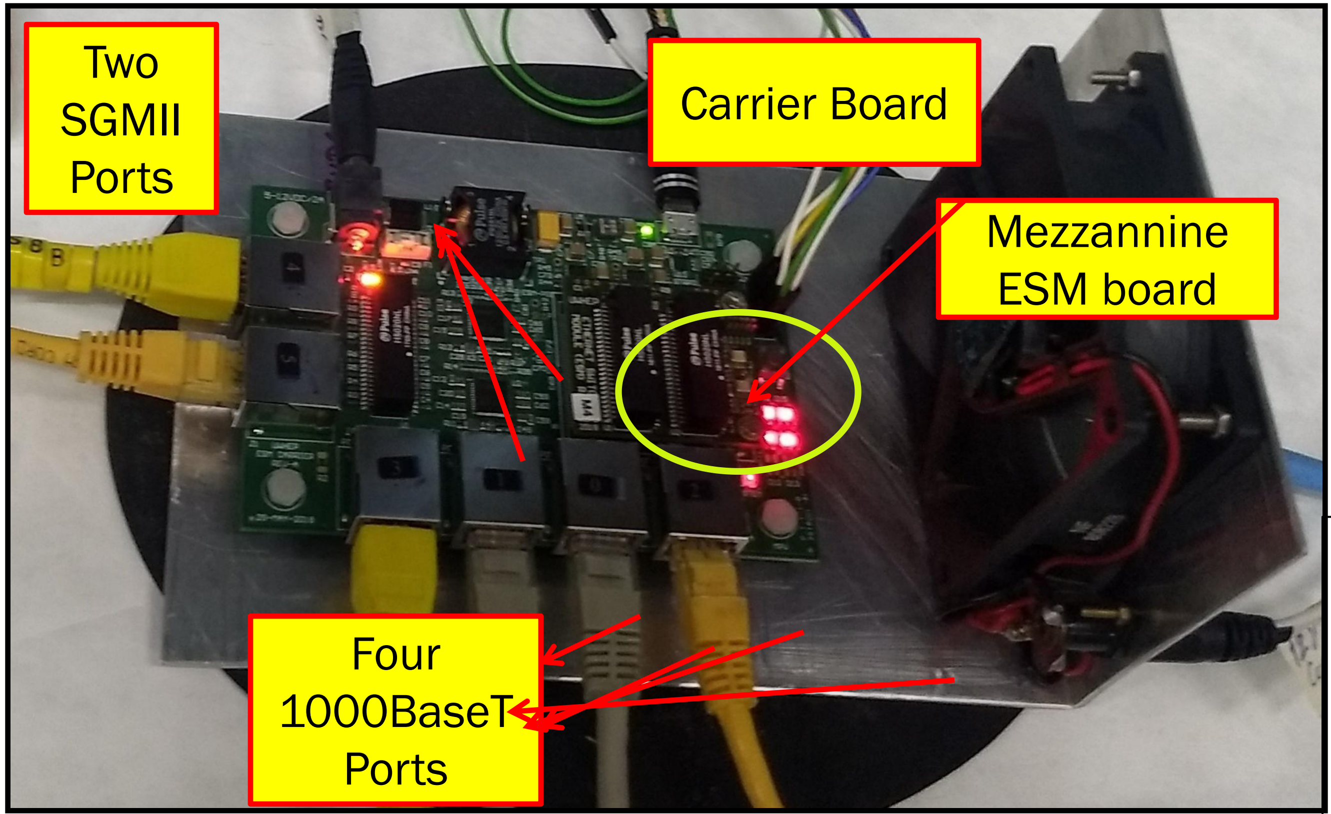
-Logging-Out of range /failure states of the system

-The IPMC is responsible for power-up and environmental monitoring of the ATCA card, including voltage and temperature.

- **Ethernet Switch (ESM)**

Connects the on-board endpoints such as the Linux & IPMC to the crate switch in an ATCA hub slot via back-plane connection (1000BASE-T is standard)

ESM (Ethernet Switch Module) test setup

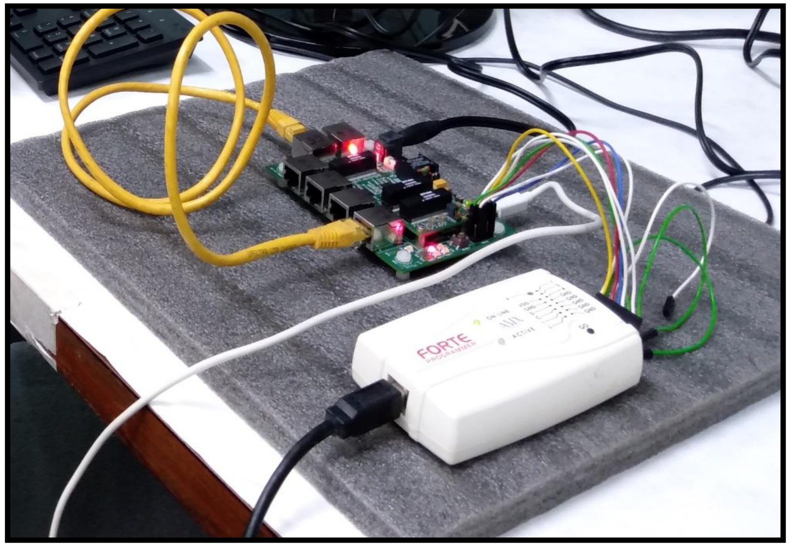


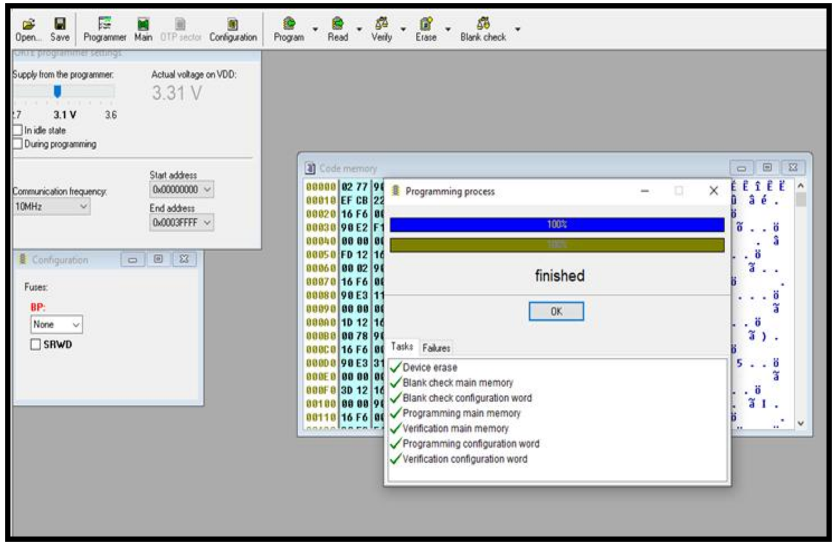
ESM BOARD MADE IN INDIA

Device similar to Ethernet hub.

- It is intelligent than hub since it remembers the physical addresses of the devices connected to it.
- Micro semi gigabit layer-2 switch:
  - Four integrated copper PHY ports
  - Two 1G SGMII ports
- +3.3V power source
- 256Kb flash on-board flash storage.
- 34x40 mm footprint

ESM firmware updating





- Asix Forte Programmer used to update the firmware(the HEX code) to the onboard switch Processor via the Flash interface

ESM test outputs

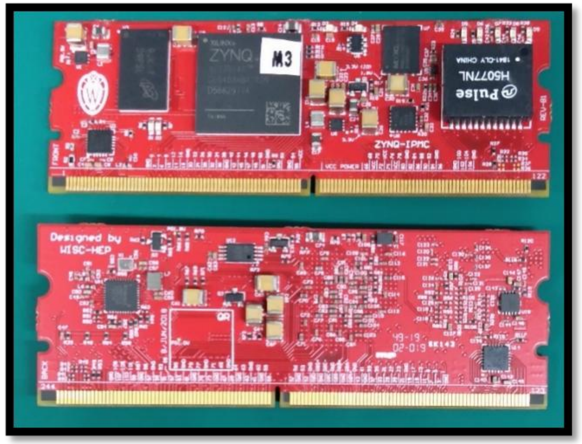
```
Chip Family      : 751x Rev.B
Software Version: Ferret_ESM_Mezz Ocelot-REL_Unmanaged
Code Revision    : 1888579
Build Date       : Apr 16 2019 14:18:17
HW Revision      : A
Strap Pins       : 3
Config record failed signature or crc check, setting def

Enter ? to get the CLI help command
>
>
>
>
>
>
>
>
>
>
>
>
>p
uPort iPort cPort MIIM Bus MIIM Addr   PHY/Serdes  CRC uPatch Link Status
-------------------------------------------------------------------------------
    1     0     0         0      0x00 FERRET_7512  No uPatch    Up - 1GFDX FC(D)
    2     1     1         0      0x01 FERRET_7512  No uPatch    Up - 1GFDX FC(D)
    3     2     2         0      0x02 FERRET_7512  No uPatch    Up - 1GFDX FC(D)
    4     3     3         0      0x03 FERRET_7512  No uPatch    Up - 1GFDX FC(D)
    5     4     7         2      0xff -            Not PHY      Up - 1GFDX FC(D)
    6     5    10         2      0xff -            Not PHY      Up - 1GFDX FC(D)
>
```

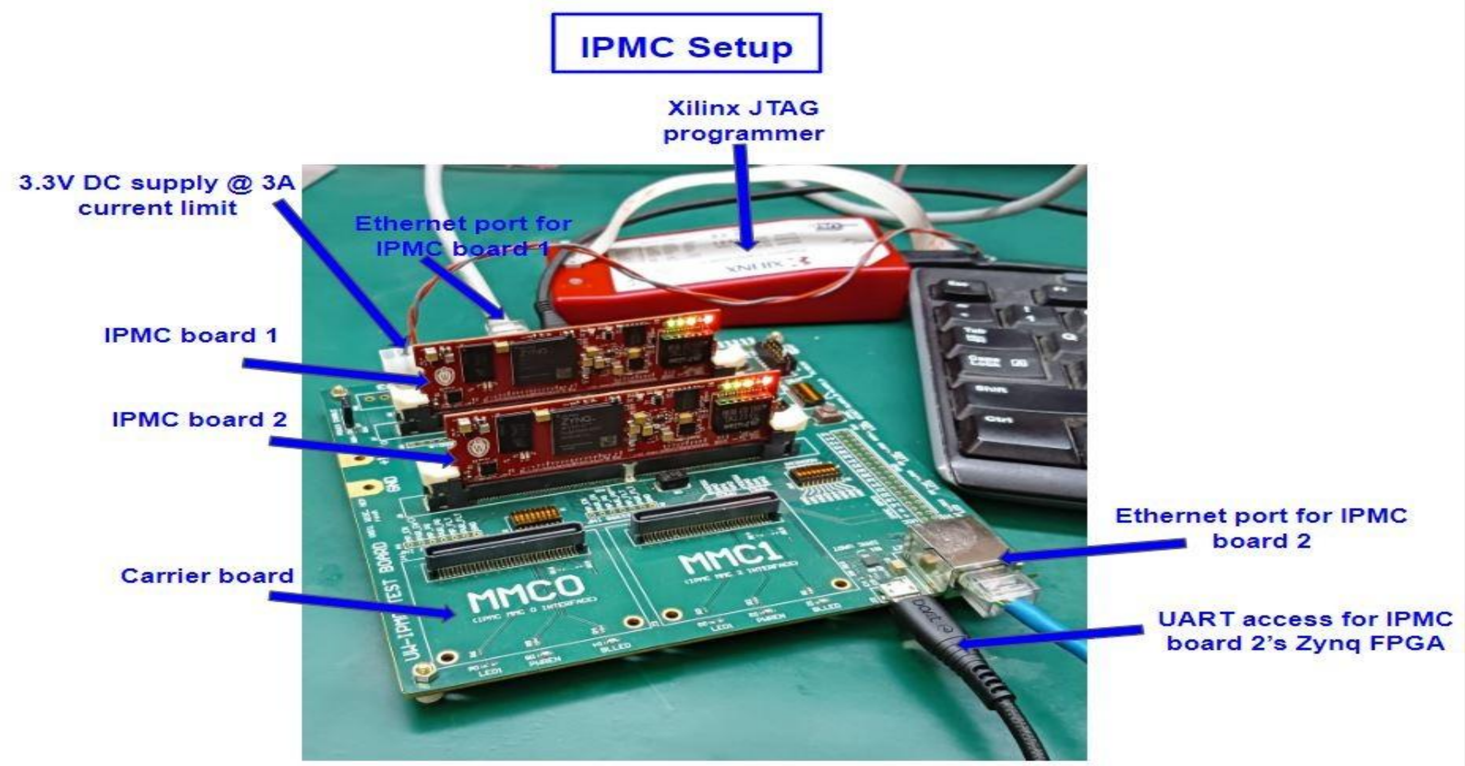
```
File  Edit  View  Search  Terminal  Help
hcal@hcal-desktop:~$ iperf3 -c 192.168.0.5 -p 5201 -P 1
Connecting to host 192.168.0.5, port 5201
[  4] local 192.168.0.3 port 45842 connected to 192.168.0.5 port 5201
[ ID] Interval           Transfer     Bandwidth       Retr  Cwnd
[  4]   0.00-1.00   sec   113 MBytes   950 Mbits/sec    0    362 KBytes
[  4]   1.00-2.00   sec   111 MBytes   935 Mbits/sec    0    380 KBytes
[  4]   2.00-3.00   sec   111 MBytes   935 Mbits/sec    0    399 KBytes
[  4]   3.00-4.00   sec   111 MBytes   935 Mbits/sec    0    399 KBytes
[  4]   4.00-5.00   sec   111 MBytes   935 Mbits/sec    0    399 KBytes
[  4]   5.00-6.00   sec   112 MBytes   936 Mbits/sec    0    419 KBytes
[  4]   6.00-7.00   sec   111 MBytes   934 Mbits/sec    0    419 KBytes
[  4]   7.00-8.00   sec   111 MBytes   934 Mbits/sec    0    419 KBytes
[  4]   8.00-9.00   sec   112 MBytes   936 Mbits/sec    0    438 KBytes
[  4]   9.00-10.00  sec   111 MBytes   935 Mbits/sec    0    438 KBytes
- - - - - - - - - - - - - - - - - - - - - - - - -
[ ID] Interval           Transfer     Bandwidth       Retr
[  4]   0.00-10.00  sec  1.09 GBytes   936 Mbits/sec    0             sender
[  4]   0.00-10.00  sec  1.09 GBytes   934 Mbits/sec                  receiver

iperf Done.
hcal@hcal-desktop:~$
```

- Each port of each board (i.e 6 ports in all) tested with loop back cables for link UP status successfully
- Each Port tested for data Bandwidth and packet loss-No packet loss found and all Ports showed activity of nearly 1GBps

IPMC (Intelligent Platform Management Controller) Boards

IPMC BOARD MADE IN INDIA





- Non-ATCA-based test fixture with some simple FPGA firmware to exercise the IPMC board and verify proper connectivity on all pins to screen the production lots, so that boards that are given to ATCA users have this first generic level of testing

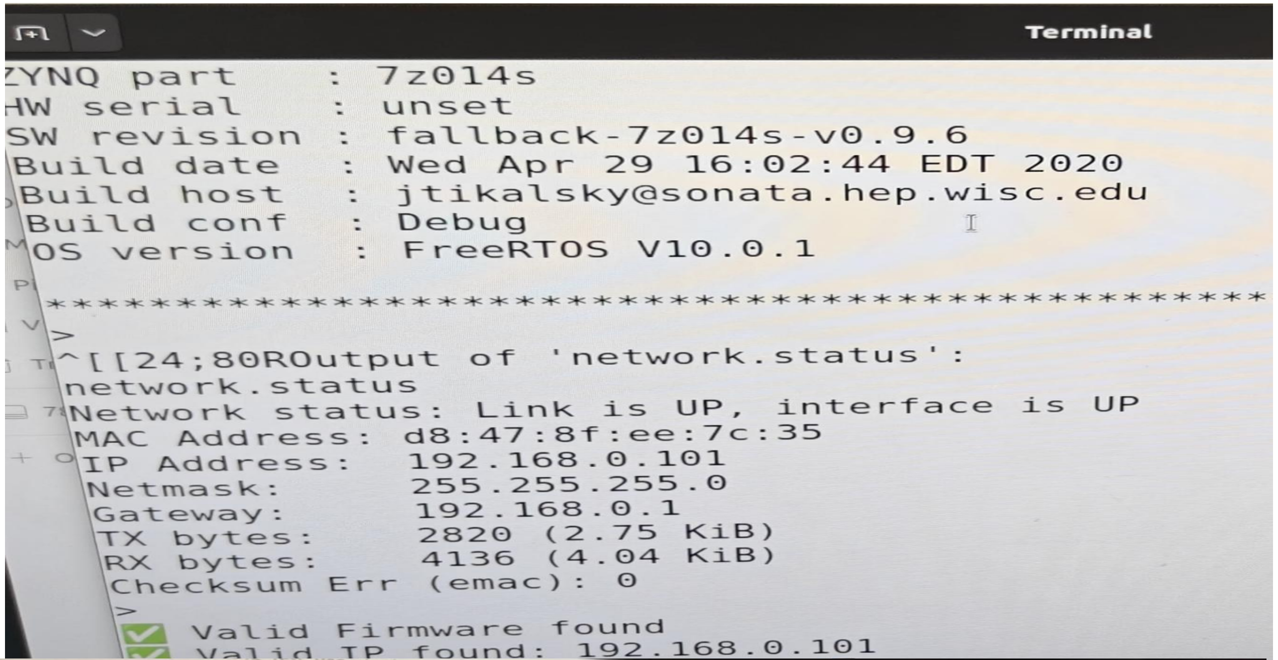
IPMC Features

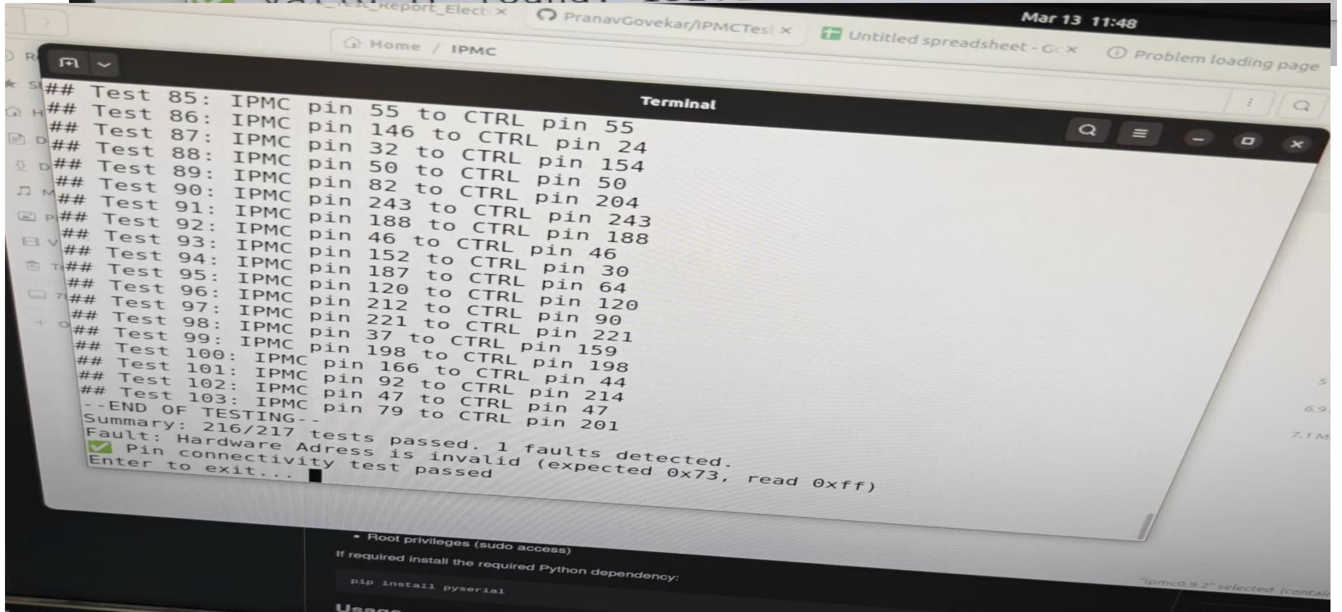
- Commercial IPMC solutions are available, but are insufficient for the APx card series, which require faster response times to faults, wider input/output options, and additional monitoring features.

- The custom IPMC is based on a Xilinx ZYNQ System-on-Chip (SoC) device in a 244-pin mini Dual In-line Memory Module (MiniDIMM) form factor
- .
- Running a Real Time Operating System (RTOS), the ARM Cortex-A series-based CPU is powerful enough to support TCP/IP connections for network-based I/O, firmware upgrades, and a Joint Test Action Group (JTAG) controller that can assist with main board debug.

- Fast ADC channels integrated with the ZYNQ programmable FPGA logic can quickly detect fault conditions on the board and support rapid intervention to prevent damage in the event of over-temperature conditions or power supply faults, including a waveform capture capability around the time of the fault.

IPMC Testing at TIFR





Trigger Algorithms and Firmware development

Development of Trigger Algorithm for HF

- The high luminosity upgrade of the Large Hadron Collider (HL-LHC) will result in significantly increased collision rates, producing about 200 simultaneous interactions per bunch crossing, known as pileup.
- To handle this, the CMS experiment will upgrade its Level-1 (L1) trigger system, using custom hardware, including FPGAs and SoMs, to process data in real-time from the tracker, high-granularity calorimeter, and other subsystems.
- Our team did develop the firmware for the incorporation of data from the Hadron Forward (HF) Calorimeter in L1 Trigger, with particle clustering and pileup mitigation achieved using the Pileup Per Particle Identification (PUPPI) algorithm

(Poster by Pranav Govekar) :Ref

Summary

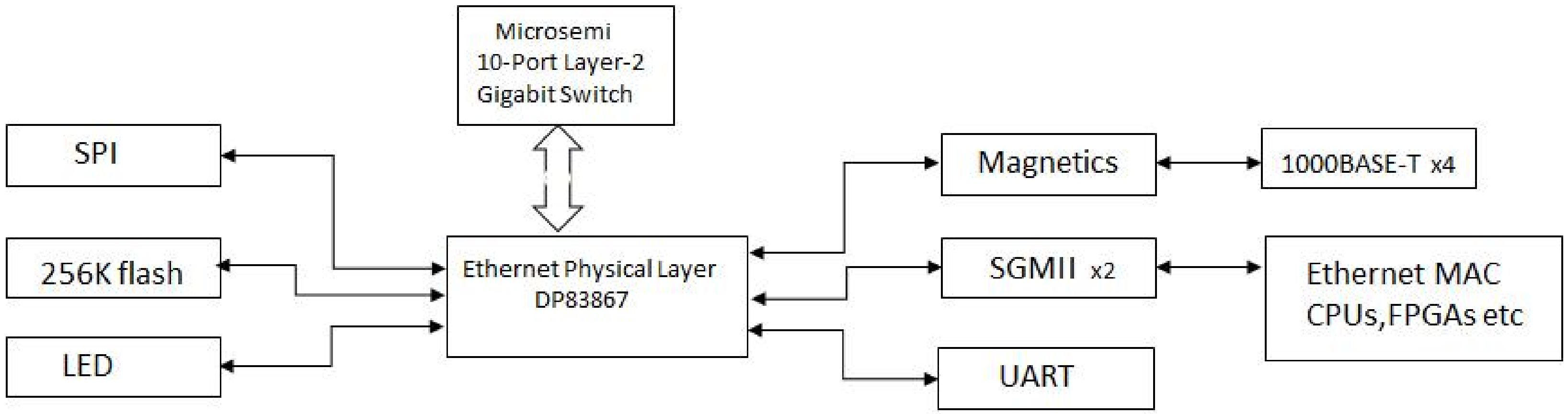
- 310 IPMC boards successfully tested at TIFR after fabrication In Indian industries (Micropack and Electrowing) and delivered to CERN
- 600 ESM boads successfully tested at TIFR after fabrication in Penisnula electronics@Bangalore and sent to CERN
- Additoonal 100 ESM boards were fabricated in Penisnula directly by CERN collaboration team and tested at TIFR
- Additional 140 IPMC boards were ordered by CERN directly with electrowing .Delivered to CERN after testing at TIFR
- Setup a stand alone test stand at CERN for testing the IPMC boards (During my recent CERN visit in Feb 2026)
- L1 Trigger HF Firmware development completed with hardware testing done

Acknowledgement to our Team

Kajari Mazumdar, M.R.Patil, Mangesh Kolwakar, Pramod Pathare, ,Pranav Govekar,Aravind S. & other EHEP colleagues

SPARE SLIDES

ESM + Carrier Board architecture



Why ATCA (Advanced Telecommunication Architecture) in HEP

The focus on high availability and reliability, the large bandwidth offered by the shelf backplane, and the large availability of electrical power and thermal dissipation make ATCA systems very attractive for use in high energy physics experiments, where extreme detector read-out rate, low latency, high availability and limited physical space occupation are requirements for the successful installation and operation of the back-end systems of the detectors.